interface
TECHNOLOGY

MP MASTER
MA25284

THIS SIDE TO SHEETS

Digitized by the Internet Archive
in 2024

https://archive.org/details/manualsplus_03936

# MODEL 553A
# USER'S MANUAL

SERIAL NO:

553A-UB-6.9
11 July, 1990

LIST OF EFFECTED PAGES

DATES OF ISSUE OF ORIGINAL AND CHANGED PAGES ARE:

| | |
|---|---|
| Original | 13 Sep, 1985 |
| Revision B | 30 Apr, 1986 |
| Revision C | 11 Jul, 1990 |

Total number of pages in this publication is 133, consisting of the following:

| Page # | Change # | Page # | Change # |
|---|---|---|---|
| Title | C | 6-1 thru 6-6 | B |
| LEP | C | A-1 thru A-9 | B |
| Change Record | C | A-10 (blank) | B |
| i thru v | C | B-1 thru B-5 | B |
| vi (blank) | B | B-6 (blank) | B |
| 1 -1 thru 1-5 | B | C-1 thru C-8 | B |
| 1-6 (blank) | B | D-1 thru D-2 | B |
| 2 -1 thru 2-13 | B | E-1 thru E-5 | B |
| 2-14 (blank) | B | E-6 (blank) | B |
| 3 -1 thru 3-3 | B | F-1 thru F-8 | B |
| 3-4 (blank) | B | G-1 thru G-35 | B |
| 4 -1 thru 4-9 | B | G-36 (blank) | B |
| 4-10 (blank) | B | H-1 | B |
| 5 -1 thru 5-5 | B | H-2 (blank) | B |
| 5-6 (blank) | B | | |

RECORD OF CHANGES

| Change No. | Date | Title or Description | Check Sum |
|---|---|---|---|
| B | 30 Apr 86 | Firmware Revision 6.9 | 50F9 |
| C | 11 Jul 90 | Replace incorrect T of C | Same |

# INTERFACE TECHNOLOGY REPAIR POLICY

All items returned to **Interface Technology** require *PRIOR AUTHORIZATION*. Authorization can be obtained through the mail, via telex (4945489), or by phone (818 914-2741). The following is subject to change without prior notice.

## WARRANTY

**Interface Technology** warrants each instrument to be free of defects in material and workmanship for a period of *ONE (1) YEAR* from the date of shipment to the original purchaser.

**Interface Technology** will, at its discretion, repair, replace or adjust any defective part or parts, free of charge, when the instrument is returned to **Interface Technology** *FREIGHT PREPAID*. .If an examination reveals that the defect has occurred because of misuse or operation under abnormal conditions, the instrument will be serviced under the *NON-WARRANTY* conditions stated below.

**Interface Technology** will return the instrument *FREIGHT PREPAID* by normal carrier (determined by **Interface Technology**). If a specific carrier is requested, shipment will be C.O.D. or billed via the carrier.

**Interface Technology** warrants their repairs to be free of defects in materials and workmanship for a period of *NINETY (90) DAYS* from the date of return shipment.

## NON-WARRANTY

Instruments returned for service after the warranty period has expired, or because of misuse or operation under abnormal conditions, will be subject to current non-warranty repair rates. Contact the factory for current repair rates and repair lead times. All shipping charges are the responsibility of the customer or the shipping party.

## FOREIGN REPAIRS

For all units shipped outside of the U.S., contact the local **Interface Technology** representative. Countries without a local **Interface Technology** representative should contact the factory directly.

# MODEL 553A MANUAL ADDENDUM

## DESCRIPTION OF FEATURES THAT DO NOT APPLY TO THE MODEL 553

This addendum applies to the Model 553 Mil-Std-1553 Bus Analyzers that have been upgraded to software revision 2.1 (SYSTEM CHECKSUM 78FF). All of the capability of the Model 553A is available as described in the Model 553A manual except for the areas noted below:

1. Encoder Memory Size

   The Model 553 contains an output (encoder) buffer of 1K microseconds of bus traffic This is enough to simulate more than a single 32 word message transaction, without loading another test number The Model 553A encoder buffer size is 4K

2. PROM Rear Panel Socket

   The Model 553 provides for PROM storage of Test Numbers that have been programmed off-line into 2716 or 2732 type PROMs. These Test Numbers can then be loaded into the Model 553 for execution from the front panel or via the remote interface. The Model 553A has been modified to support writing to an EEPROM plugged directly into the rear panel socket. This provides local non-volatile Test Number storage. Note that the location of pin 1 has been changed in the Model 553A.

3. Front Panel Keyboard Labels

   The Model 553 software revision 2.1 includes several features that are accessed using "shifted key" functions. While these are not labeled on the Model 553 front panel, they can still be selected, just as in the Model 553A. These keys are:

   RESET (Shift, 9): This resets all ramp functions back to their initial conditions.

   BK DIR (Shift, A): When in the Active Block, this will provide a listing of all the Test Numbers stored in the internal RAM and the external PROM socket.

   BK DSP (Shift,2): When in the Active Block, this will display the contents of the specified Test Number, without overwriting the present Active Block.

   SAV EE (Shift,2): This is not functional.

   FMT EE (Shift, 3): This is not functional.

4. Remote Commands

   There are two remote commands associated with the EEPROM program storage that are not valid for the Model 553. These commands are:

   SE: Save block to EEPROM
   FM: Format EEPROM

5. Internal Memory Size

   The Model 553 has an Active Block size of 1K for the creation of Test Blocks, and 5K of RAM for the storage of multiple Test Numbers. This compares with a 2K Active Block and 13K of RAM for Test Number storage in the Model 553A.

6. Circuit Card Assembly Numbers

   The Drawing and Assembly numbers listed in the Model 553A manual do not apply to the Model 553, and are not compatible. Contact the Service Department for any repair or replacement requirements.

# Table of Contents


| Section | Description | Page |
|---|---|---|
| 1.0 | Introduction | 1-1 |
| 1.1 | General | 1-1 |
| 1.2 | Features | 1-1 |
| 1.3 | Architecture | 1-1 |
| 1.4 | Basic Programming | 1-3 |
| 1.5 | Operating Modes | 1-3 |
| 1.5.1 | BC Simulator | 1-3 |
| 1.5.2 | RT Simulator | 1-4 |
| 1.5.3 | Bus Monitor | 1-4 |
| 1.6 | Technical Specifications | 1-4 |
| 2.0 | Programming | 2-1 |
| 2.1 | Menu Parameters | 2-3 |
| 2.1.1 | Configuration Menu | 2-3 |
| 2.1.2 | Transmitter Menu | 2-4 |
| 2.1.3 | Transmitter Amplitude | 2-4 |
| 2.1.4 | Transmitter Zero-Crossing | 2-5 |
| 2.1.5 | Receiver Menu | 2-6 |
| 2.1.6 | Control Menu | 2-6 |
| 2.1.7 | Trap Menu | 2-8 |
| 2.1.8 | Active Data Block Menu | 2-9 |
| 2.2 | Data Block Programming | 2-10 |
| 2.2.1 | Editing And The Active Block | 2-10 |
| 2.2.2 | Data Programming | 2-10 |
| 2.2.3 | Error Generation | 2-10 |
| 2.2.4 | Gaps (Dead Line Time) | 2-11 |
| 2.2.5 | Program Control Words | 2-11 |
| 2.2.5.1 | GOSUB | 2-11 |
| 2.2.5.2 | GOTO | 2-11 |
| 2.2.5.3 | PAUSE | 2-11 |
| 2.2.5.4 | PRINT | 2-12 |
| 2.2.5.5 | STORE | 2-12 |
| 2.2.6 | Saved Blocks | 2-12 |
| 2.2.7 | General Considerations And Limits | 2-13 |
| 2.2.8 | Ramp Reset | 2-13 |
| 2.3 | Remote Interface | 2-13 |
| 3.0 | Data Display | 3-1 |
| 3.1 | Display Device Selection | 3-1 |
| 3.2 | Display Format | 3-1 |
| 4.0 | Rear Panel Signals | 4-1 |

| Section | Description | Page |
|---|---|---|
| 4.1 | MIL-STD-1553 Bus Connectors | 4-1 |
| 4.2 | Transmitter Sync Output | 4-1 |
| 4.3 | Trap Detect Output | 4-1 |
| 4.4 | External Trigger Input | 4-1 |
| 4.5 | PROM/EEPROM Socket | 4-1 |
| 4.6 | RS-232C | 4-1 |
| 4.6.1 | Clear To Send (CTS) | 4-5 |
| 4.6.2 | Data Set Ready (DSR) | 4-5 |
| 4.6.3 | Request To Send (RTS) | 4-5 |
| 4.6.4 | Data Terminal Ready (DTR) | 4-5 |
| 4.6.5 | "RT Ready" Handshake | 4-5 |
| 4.7 | IEEE 488 | 4-5 |
| 4.7.1 | IEEE 488 Functions | 4-7 |
| 4.8 | Composite Video | 4-9 |
| 5.0 | Self Test | 5-1 |
| 5.1 | CPU Tests | 5-1 |
| 5.2 | Encoder Tests | 5-2 |
| 5.3 | Decoder Tests | 5-3 |
| 6.0 | Installation And Maintenance | 6-1 |
| 6.1 | Unpacking And Inspection | 6-1 |
| 6.2 | Mechanical Installation | 6-1 |
| 6.3 | Electrical Installation | 6-1 |
| 6.4 | Functional Verification | 6-2 |
| 6.4.1 | Self Test | 6-2 |
| 6.4.2 | Bus Coupling Test | 6-3 |
| 6.4.3 | Transmitter Amplitude Calibration | 6-5 |
| 6.4.4 | Zero-Crossing Deviation Test | 6-5 |

# Appendices


| Appendix | | Description | Page |
|---|---|---|---|
| A | | Programming Syntax | |
| | A.1 | Notation | A-1 |
| | A.2 | Programming Syntax | A-1 |
| | A.2.1 | Block Commands | A-3 |
| | A.2.2 | Runtime Commands | A-7 |
| | A.3 | Pre-programming A PROM | A-9 |
| B | | Examples | B-1 |
| C | | Options For 553A Output | C-1 |
| D | | Model 553A Data Entry Error Codes | D-1 |
| E | | Self Test Glossary And Error Displays | E-1 |
| F | | Coding Forms | F-1 |
| | F.1 | Model 553A Command Word Coding | F-2 |
| | F.2 | Model 553A Data Word Coding | F-4 |
| | F.3 | Model 553A Status Word Coding | F-6 |
| G | | 553A Theory Of Operation | |
| | | CPU Theory Of Operation | G-1 |
| | | CPU Detailed Circuit Description | G-1 |
| | | Decoder Theory Of Operation | G-11 |
| | | Decoder-Detailed Circuit Description | G-13 |
| | | Encoder Theory Of Operation | G-23 |
| | | Encoder-Detailed Circuit Description | G-25 |
| H | | Schematics | H-1 |

# List of Figures


| Figure # | Description | Page |
|---|---|---|
| 1.1 | Model 553A Block Diagram | 1-2 |
| 2.1 | Model 553A Front Panel And Display | 2-2 |
| 4.1 | Model 553A Rear Panel Connectors | 4-2 |
| 6.1 | Manchester Waveform | 6-6 |
| 6.2 | Zero-Crossing Display | 6-6 |
| 6.3 | Zero-Crossing Calibration | 6-6 |
| 1A | 1553A Direct Coupled To A Bus | C-2 |
| 2A | 1553A Transformer Coupled To A Bus | C-3 |
| 3A/4A | 1553A Coupling To An Instrument Or LRU | C-4 |
| 1B | 1553B Direct Coupled To The Bus | C-5 |
| 2B | 1553B Transformer Coupled To The Bus | C-6 |
| 3B | 1553B Direct Coupled To An Instrument Or LRU | C-7 |
| 4B | 1553B Transformer Coupled To An Instrument Or LRU | C-8 |
| 1 | CPU Block Diagram | G-2 |
| 2 | Decoder Block Diagram | G-12 |
| 3 | Memory Access Timing | G-18 |
| 4 | Sample Trap Circuit Timing | G-21 |
| 5 | Memory Access VS. Trap Timing | G-22 |
| 6 | Encoder Block Diagram | G-24 |
| 7 | Encoder Start / Stop Timing | G-27 |
| 8 | Encoder Bit Timing | G-31 |
| 9 | Timing Of Zero-Crossing Adjust Shown With $V_{zw5}$ Set For 0 Deviation | G-34 |

# List of Tables


| Table # | Description | Page |
|---|---|---|
| 3.1 | Special Display Characters | 3-2 |
| 3.2 | Memory Dump Status Byte | 3-3 |
| 4.1 | RS-232 Baud Rate Settings | 4-3 |
| 4.2 | RS-232 Pin Connections | 4-4 |
| 4.3 | IEEE 488 Supported Modes | 4-6 |
| A.1 | ASCII Character Codes | A-2 |
| E.1 | Error Display Descriptions | E-2 |
| 1 | Intercard Connector Pin Assignments | G-3 |
| 2 | CPU Memory Map | G-5 |
| 3 | Input And Output Port Definitions | G-6 |
| 4 | Options For 553A Output Menu Selection | G-29 |
| 5 | Relay Matrix For All Options | G-30 |

# 1.0 INTRODUCTION

## 1.1 GENERAL

The Interface Technology Model 553A is for use in developing, testing, and troubleshooting equipment and systems which interface with MIL-STD-1553A/B data communication buses. It may provide the MIL-STD-1553A/B signal generation and verification in a manual or automated test system. It is capable of operating as a bus controller, remote terminal or bus monitor. Errors on the bus are detected or may be intentionally generated to determine the response of equipment under test. The Interface Technology Model 553A is a compact portable instrument meeting the need for an economical MIL-STD-1553 data bus tester in bench top or rack mounted applications.

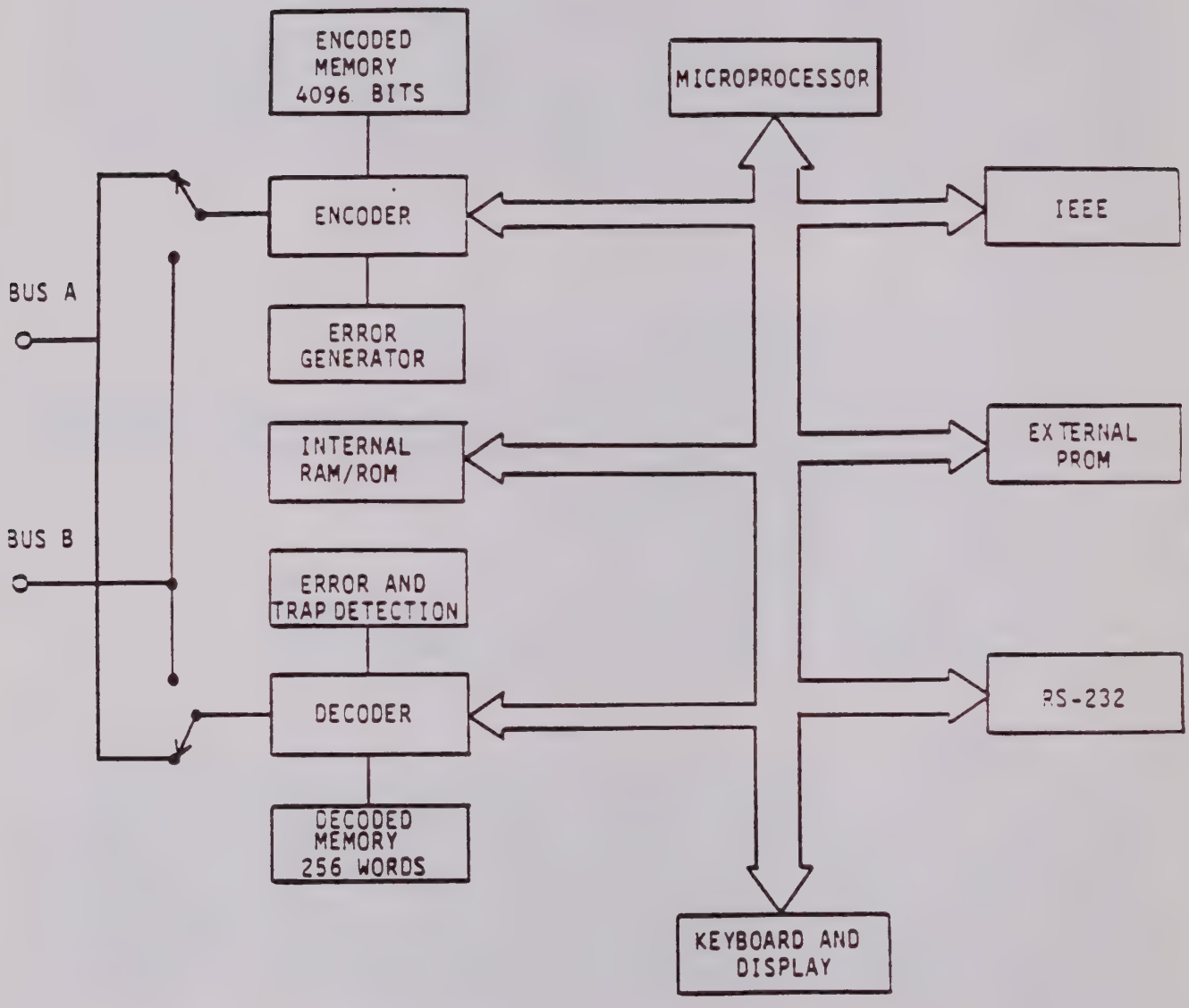
## 1.2 FEATURES

- o MIL-STD-1553 A/B compatible
- o Bus Control, Remote Terminal and Monitor modes
- o Error generation and detection capabilities
- o Print output function available
- o Ideal for development engineering, evaluation/incoming inspection testing, production testing and maintenance and repair application
- o Sinusoidal Transmitter Output
- o Variable Ramp Transmitter Amplitude
- o Variable Ramp Zero Crossing Deviation
- o Variable Slow Trigger Rate
- o Remote Readback of Menu Setup
- o Remote Readback of Test Blocks Directory of RAM, PROM
- o Remote Readback of Active or Test Blocks from RAM, PROM

## 1.3 ARCHITECTURE

Figure 1.1 presents a block diagram of the Model 553A analyzer. Operation is controlled via a microprocessor which accepts operator inputs from either the front panel, IEEE or RS-232. Similarly, results may be read out on the CRT or over the IEEE or RS-232 interface. Messages to be transmitted are entered by the operator, or accessed from a previously programmed ROM, and stored in internal RAM. Upon RUN, the internal RAM information is processed and stored into the encoded memory. The encoded memory contains the storage for 1024 bit times or cells of information. While running, the encoded memory is accessed each microsecond to generate the next cell of information.

FIGURE 1.1. MODEL 553A BLOCK DIAGRAM



The decoded memory contains storage for up to 256 words of received data. Gaps are treated as a single word on the bus with null contents. The operator has control over what is stored in the decoded memory via a trap word specification. No trap word, i.e. trap on anything, will cause the first 256 words to be stored. Entry of a specific trap word will cause the data before, centered or after the receipt of the trap word to be stored for later analysis.

## 1.4 BASIC PROGRAMMING

All of the functions of the Model 553A may be fully controlled in any of three ways: manually, through the RS-232 port, or through the IEEE 488 port. The RS-232 and IEEE 488 are referred to as the automated interfaces in that the Model 553A can be operated by a computer or controller through either one. Manual or automated control may be combined in various ways.

The relatively fixed operating parameters (e.g. bus selection, signal amplitude, data and display format, etc.) are programmed through a menu. The manually operated menu permits an operator with little or no experience to set these parameters. Simple commands set menu parameters through the automated interfaces.

Data consisting of command/status/data words and gaps are programmed into blocks. Data programming and editing is through the active block (accessed by the ENTER key). Other blocks are stored in RAM or PROM and are identified by a test number. If a word is to be transmitted with an error, the error is defined along with the word in the block. Program control words may be entered into a block to permit sequences of tests (blocks) to be chained together and run automatically.

## 1.5 OPERATING MODES

### 1.5.1 BC SIMULATOR

The Model 553A is ideally suited to perform bus controller functions to test remote terminals. Command and data words are programmed into blocks. When executed, the active block is transmitted and the response displayed. Each block is assigned a test number by the user and may either be stored in memory (RAM) or programmed into EPROM/EEPROM. Previously programmed tests are recalled by their test number for execution or editing.

### 1.5.2 RT SIMULATOR

A sequence of status and data words is programmed into the active block. When enabled, the Model 553A monitors the bus until a specified trap condition is detected. The active block is then transmitted and the transaction is displayed.

### 1.5.3 BUS MONITOR

The Model 553A may be used like a logic analyzer to monitor activity on the bus. A trap word, set in the menu and also used in the RT mode, triggers the display. A total of 256 words, including gaps, may be displayed following, preceding or centered on the trap word. The trap word is a single word with don't care, sync, and data bits. Additionally, the trap may be ORed with an error causing the display to trap on the first occurrence of the trap word or an error.

## 1.6 TECHNICAL SPECIFICATIONS

**General**

| | |
|---|---|
| Protocol: | MIL-STD-1553A<br>MIL-STD-1553B |
| Modes: | Bus Controller<br>Remote Terminal<br>Bus Monitor |
| Control: | Manual - Keyboard and CRT Display<br>RS-232C<br>IEEE 488 |
| Keyboard: | 28 Key Switches |
| CRT Display: | 5 Inch Diagonal<br>32 Characters/Line<br>16 Lines |
| RS-232C: | Baud Rate: 150, 300, 600, 1200, 2400, 4800, 9600, 19200<br>Parity: None<br>Data Bits: 8<br>Stop/Start Bits: 1 |
| User Memory: | RAM: Approximately 13K Characters<br>PROM: User Supplied<br>2716 and 2732 Pin Compatible, Up to 4K Characters<br>EEPROM: 2816 Pin Compatible, Up to 2K Characters |
| Number Base: | Octal or Hexadecimal |

MIL-STD-1553

| | |
|---|---|
| Detectable Errors: | Sync, Word Length, Manchester, Parity, Continuity |
| Generatable Errors: | Sync, Word Length, Manchester, Parity, Continuity, Zero Crossing |
| Zero Crossing: | Mid Bit or End of Bit<br>Selectable to Any Bit<br>Settable within Range ±375 ns., with Resolution of 3 ns. over ±300 ns. |
| Transmitted Amplitude: | 27 Vpp (1553B Transformer Coupling)<br>20 Vpp (1553A Transformer Coupling)<br>Settable 0 to 100% with Resolution of 0.4% |
| Encoder Capacity: | Transmitted sequence of words and gaps up to 1024 microseconds. |
| Decoder Capacity: | 256 words including gaps. |
| Bus Interface: | Two Trompeter BJ77 connectors. Encoder and decoder independently switchable to either connector. |
| External Trigger Input: | TTL low going edge starts encoder.<br>BNC connector. |
| Transmitter Sync Output: | TTL active low during encoder sequence.<br>BNC connector. |
| Trap Detect Output: | TTL active low 0.25 microsecond pulse after a trap detect.<br>BNC connector. |

Physical and Power Requirements

| | |
|---|---|
| Size: | 5.2" H x 19" W x 19" D (132 mm x 483 mm x 483 mm)<br>17" (432 mm) Behind Rack Panel |
| Weight: | Approximately 22 lbs. (10 kg) |
| Operating Temperature: | 0° to 50° C. |
| Power Requirement: | 90-132 VAC<br>180-264 VAC<br>47-440 Hz<br>80 Watts Maximum |

## 2.0 PROGRAMMING

Programming the Model 553A may be accomplished via the front panel display and switches (see Figure 2.1) or from a remote interface via RS-232 or IEEE 488. Appendix A provides the exact syntax for remote programming. Appendix B provides examples of program set-ups for both front panel and remote operation.

The essential method of operation is as follows:

1. Select the Desired Mode. The current mode is displayed on the topmost line of the CRT and is modifiable when displayed in reverse video (accomplished via MENU key). Successive depressions of the NEXT key will cycle through the mode alternatives:

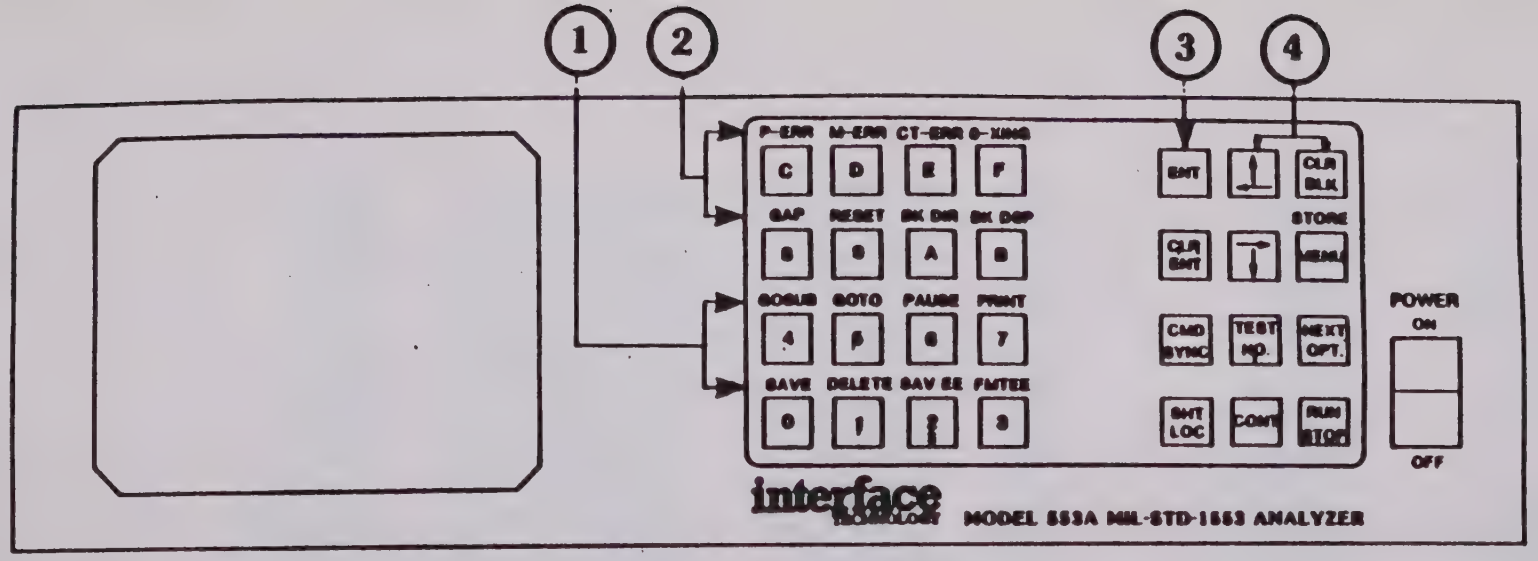
   - o BC Simulator
   - o RT Simulator
   - o Monitor
   - o Self Test

   Once the desired mode is displayed via the NEXT key, depression(s) of the MENU key will cycle through all the relevant menus for the selected mode.

2. Establish Desired Operating Parameters. By the depression of the MENU key, the different pages of optional parameter set-ups will be displayed. As before, a parameter field is modifiable when it is being displayed in reverse video (accessed via cursor keys ↑, →, ←, ↓). The various options are selected via the NEXT key which will display the next valid alternative upon each depression.

3. Program the Data Block. Depressing the ENTER key will display the active (current) data block to be transmitted and allows for further data entry/editing. As data is entered, it is displayed on the last line of the CRT until ENTER is depressed. At that time, the data is removed from the input line and placed in the active block at the location designated by the cursor (reverse video). Editing may occur by positioning the cursor as desired (↑, →, ←, ↓) and simply making a new entry. A null entry (ENTER key alone) will delete the cursored entry.

   When building up the active block with a combination of messages and test numbers, it is helpful to examine a previously saved test. This can be done by using the BK DIR (block directory) and BK DSP (block display) shifted key functions.




(1) Program Control Functions: Accessed via SHIFT followed by appropriate hexadecimal key entry.

(2) Bus Error Functions: Accessed via SHIFT followed by appropriate hexadecimal key entry. Allows forced generation of a parity error (P-ERR), manchester error (M-ERR), count error (CNT-ERR), zero crossing deviation (0-XING), and/or gap time (GAP).

(3) Entry Control: Single action keys for the following:

ENTER: Follows numerical entries to signal completion. When used without prior numerical entry, displays active block being processed for encoder.
CLEAR ENTRY: Clears an input prior to ENTER.
CMD SYNC: Used prior to data entry to indicate next word shall be a command/status word transmission. Indicated on the CRT by the letter "K".
SHIFT/LCL: SHIFT allows access to Program Control and Bus Error functions. Secondarily, if in Remote lockout, causes unit to return to local.

(4) Display Control

UP/LEFT & DOWN/RIGHT CURSOR: Used to move cursor (reverse video) through field selections and data.
TEST NO.: Used to recall a previously saved block for display/editing.
CONT: Used as a "continue" function in response to a "pause" instruction. When used alone, recalls the current state of the decoder memory (received) for display.
CLEAR BLOCK: An editing function used to clear the entire block being displayed.
MENU: Changes CRT display from menu to menu.
NEXT: Selects the next valid parameter for the given field (reverse video). Successive depression cycles through all options.
RUN/STOP: Alternate action key used to start a cease program execution.

FIGURE 2.1. MODEL 553A FRONT PANEL AND DISPLAY

From the active block a directory of all test numbers stored in RAM and PROM is provided by the BK DIR key. After it has been viewed, pressing the ENTER key returns to the active block. These functions are supported for the Model 553A even though the keyboard is not labeled.

An individual test block can be viewed by selecting the BK DSP key and entering the appropriate block number. This mode is for display only, and will not allow data to be modified. Pressing the ENTER key will return to the active block.

4. Run the Created Program. When all entries have been made and programmed as desired, simply depress the RUN/STOP key. The upper right hand display of the CRT will display "RUN", "STOP", or "ERROR XX". If an error code appears, it must be resolved before the actual RUN state will occur. Appendix D provides a listing of the error codes and their meaning.

## 2.1 MENU PARAMETERS

The following subparagraphs describe the various menu pages and their applicable parameter fields.

### 2.1.1 CONFIGURATION MENU

Applicable modes: BC Simulator, RT Simulator, Monitor.

| Parameter | Alternatives | Description |
|---|---|---|
| Simulate Bus | Yes or No | User selects whether Model 553A has the 1553A/B Bus internal to it or external to it. If simulated, the Model 553A has an internal parallel load resistor included; refer to Appendix C for details. |
| Coupling | Direct or Xformer | User selects ratio of transformer taps to connect to the 1553A/B bus; refer to Appendix C for details. |
| Protocol | 1553B or 1553A | Specifies which standard is to be applied for the data bus interface. See Appendix C for details. |

## 2.1.2 TRANSMITTER MENU

Applicable modes: BC Simulator and RT Simulator.

| Parameter | Alternatives | Description |
|---|---|---|
| Bus | A or B | User selects transmission on on A or B bus at rear panel. |
| Trigger | Internal or External | User selects triggering to occur external via rear panel connector or internally. |
| Manchester Cell Override | 00, 01, 10 or 11 | User can specify polarity of each half of a bit time for Manchester error. A "00" or "11" will cause both half cells to low or high without any mid bit transition and therefore a Manchester error. |

## 2.1.3 TRANSMITTER AMPLITUDE

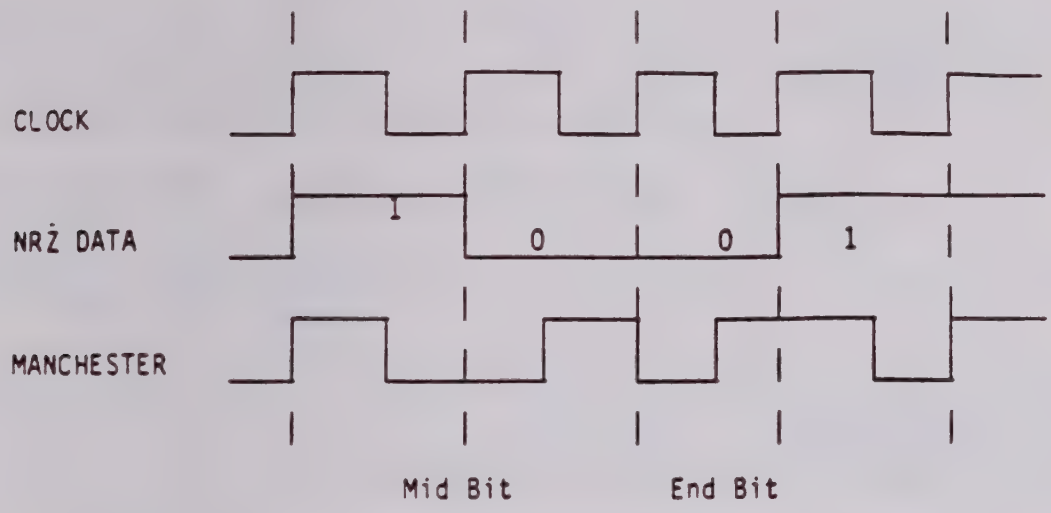
Applicable modes: BC Simulator and RT Simulator (Ramp function can only be used with Variable Trigger Rate).

| Parameter | Alternatives | Description |
|---|---|---|
| Selection | Fixed or Ramp | Defines amplitude as Fixed or Ramp. There will be an Error 19 if Zero Crossing Ramp is simultaneously selected. |
| Fixed Amplitude | Full, Adj or Set | Defines Fixed Amplitude. |
| Ramp Upper Limit | Adj or Set | Defines Amplitude Upper Ramp limit. |
| Ramp Lower Limit | Adj or Set | Defines Amplitude Lower Ramp Limit. |
| Ramp Type | 0 Cycle on Lower Limit<br>1 Cycle on No Response<br>2 Hold on Lower Limit<br>3 Hold on No Response<br>4 Stop on Lower Limit<br>5 Stop on No Response | Defines type of ramping. |

## 2.1.4 TRANSMITTER ZERO CROSSING

Applicable modes: BC Simulator, RT Simulator (Ramp function can only be used with Variable Trigger Rate).

| Parameter | Alternatives | Description |
|---|---|---|
| Bit Position | Mid or End Bit | Define Position of Zero Crossing |




| | | |
|---|---|---|
| Selection | Fixed or Ramp | Define Fixed or Ramp Zero Crossing. There will be an Error 19 if Ramp Amplitude is simultaneously set. |
| Fixed Deviation | Zero, Adj or Set | Define Deviation Error +375 ns with 3 ns Resolution. |
| Ramp Limit | Adj or Set | Define Absolute Deviation Limit. |
| Ramp Direction | Pos, Neg or +&- | Define Ramp Direction. |
| Ramp Type | 0 Cycle on Limit<br>1 Cycle on No Response<br>2 Hold on Limit<br>3 Hold on No Response<br>4 Stop on Limit<br>5 Stop on No Response | Defines Ramping Type. |

### 2.1.5 RECEIVER MENU

Applicable modes: BC Simulator, RT Simulator, Monitor.

| Parameter | Alternatives | Description |
|---|---|---|
| Bus | A or B | User selects receiving data on A or B bus at rear panel connector. |
| Display with Xmit Data | Yes or No | Yes-The receiver is enabled continuously while running. Transmitted data is received and displayed.<br><br>No-The receiver is disabled while the transmitter is active. Only data received from external device is displayed. See example 18 in Appendix B. |

### 2.1.6 CONTROL MENU

Applicable modes: BC Simulator, RT Simulator, Monitor.

| Parameter | Alternatives | Description |
|---|---|---|
| Trigger Rate | Step, Fast Repeat, or Variable Repeat | STEP: The test is run once and then stopped.<br><br>FAST REPEAT: The test is continuously repeated at a high rate. The operation for the different modes is noted below. Note that once the encoder is loaded and ready to transmit, no further processing of program control functions (e.g. GOTO, GOSUB) occurs. The encoder is placed in a tight loop always ready to transmit that first set of data.<br><br>VARIABLE REPEAT: Allows a programmable time interval to be specified from 0-1000 ms for generating a repeatable trigger. The time between multiple test messages will be the programmed repeat time interval, plus set-up and test execution time. |

Trigger Rate (continued)

Notes on FAST REPEAT Trigger Rate:

BC MODE: With the transmitter trigger set to INTERNAL, the contents of the encoder memory is transmitted repeatedly with a minimum loop-back time to the first word of approximately 15 microseconds. It is recommended that only step or variable repeat be used when printing to the CRT or a remote interface. With the transmitter trigger set to EXTERNAL, the contents of the encoder memory is transmitted each time the external trigger is received.

In the following example, the Model 553A is simulating a bus controller and is set on FAST REPEAT. The data string entered into the active block would consist of two sections: the actual transmit message, and a gap time programmed to allow the RT response to be received before repeating the transmit message.

| K1111 2222 3333 | GP32 | K4444 5555 6666 | GP32 | ... |
|---|---|---|---|---|
| BC Message #1 | RT Response | BC Message #2 | RT Response | |

RT MODE: The encoder contents are transmitted in response to each trap detect that is received.

MONITOR MODE: The Model 553A will wait for a trap, receive data for an additional 4.096 ms and then repeat by looping back, clearing the receive buffer, and waiting for another trap. It is recommended that only step or variable repeat be used when printing to the CRT or a remote interface.

| | | |
|---|---|---|
| Display Format | Abbrev, Full, or | The data displayed may be in one of the following formats: Abbrev means a listing horizontally of the data to be displayed and an indication of the highest priority error; Full means listed vertically and includes all errors detected for that word. Full format also displays measured dead line times up to 32 microseconds. Dump means list the decoded memory data vertically in straight hexadecimal, in a fixed format useful for remote analysis. |
| Input Numbers | Hex or Oct | User selects Hex or Octal input. |
| Display Numbers | Hex or Oct | User selects Hex or Octal display. |

| | | |
|---|---|---|
| Display Numbers | Hex or Octal | User selects Hex or Octal display. |
| Print Device | CRT, IEEE, RS-232 or NONE | If a print statement occurs, this selection will specify the device that the data will be sent to. |

### 2.1.7 TRAP MENU

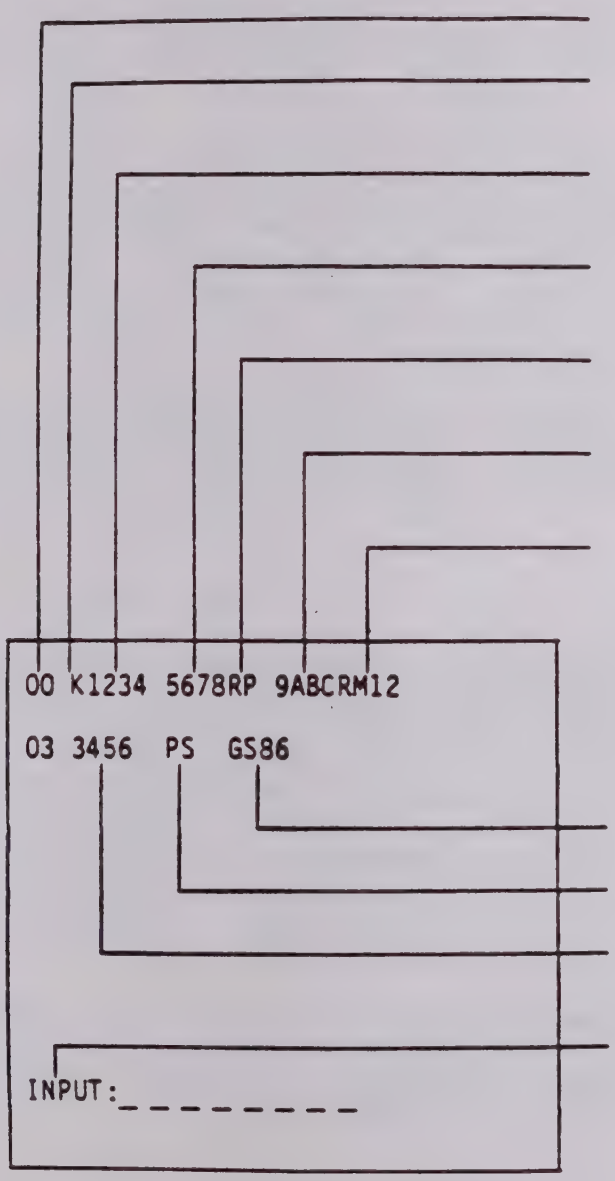
Applicable modes: RT Simulator and Monitor.

| Parameter | Alternatives | Description |
|---|---|---|
| Sync | Command, Data or Don't Care | Search for command sync pattern, data sync pattern or don't care. |
| Binary Data | Adj or Set | User can define the 16 bits of the command or data word to compare against; cursor keys and 1, 0, X(2) can be used to enter when Adj is selected; data can be Set using NEXT key. |
| Hex Data | Adj or Set | User can define the 4 Hex characters representing the 16 binary bits of the command or data word to compare against; keys 0 through F are entered and automatically converted for both the binary display and hex display. |
| Trap On | Anything, Word Only, Word or Error, or Error Only | Allows user to select what will cause trigger; "anything" means start immediately; "word only" implies trigger only on what was set up above; "error" indicates when any detectable error occurs. |
| Display | Post-Trig, Pre-Trig, or Centered | Used to select whether display memory is after the trigger event, before the trigger event or if the trigger is centered in the 256 word memory. Applicable to Monitor mode only. |

## 2.1.8 ACTIVE DATA BLOCK MENU

Applicable modes: BC Simulator and RT Simulator (Monitor mode when printing to a remote interface).

This menu has no parameter fields as such since it is used to input the desired command/data/status words to be transmitted and control thereof. It is accessed via the ENTER key without an intervening input. A example active block display is given below:




Word count or instruction numbers.

K = command sync (as opposed to data sync).

1234 = 16 bit word represented as four hex characters.

5678 = data word, 16 bits represented by four hex characters.

RP = this word shall have parity error.

9ABC = data word, 16 bits represented by four hex characters.

RM12 = this word shall have a Manchester error inserted at bit 12.

Go to subroutine 86 command.

Pause command.

Standard data word without errors.

Input section, all keyboard entries are displayed here prior to ENTER button.

## 2.2 DATA BLOCK PROGRAMMING

Tests consisting of data to be transmitted and various control information is programmed into and stored in blocks. The current block being defined or executed is called the active block. All other blocks are stored in memory and are identified by a test number.

### 2.2.1 EDITING AND THE ACTIVE BLOCK

All input and editing of block information is done through the active block while in the input state. The input state is entered automatically when a block word is received over one of the automated interfaces, or manually when the ENTER key is pressed.

Block words are keyed in an input line. After a block word is entered, pressing the ENTER key causes the word to be moved from the input line up into the active block at the location of the cursor. While in the input state, the pointer keys move the cursor within the active block. Displayed as reverse video, the cursor can be moved onto or between words. This permits words to be replaced or inserted into the active block. With the cursor on a word and with an empty input line, an ENTER command deletes the word.

The input line is cleared automatically after an ENTER command or manually using the CLEAR ENTRY key. The information in the active block is lost only when a CLEAR BLOCK command is issued or when replaced by a previously stored bloc using the "TEST NO." command.

### 2.2.2 DATA PROGRAMMING

Any normal MIL-STD-1553 data word is defined by the sync polarity and sixteen bits of data. The Model 553A defaults to a data sync unless a command sync is specified using the "CMD SYNC" key. The data bits are specified using four hexadecimal or six octal characters. The parity bit is automatically set for odd parity unless a parity error is requested. In manual operation, delimiters are placed between words when the ENTER key is pressed. In automated operation, a delimiter performs the same function as pressing the ENTER key.

### 2.2.3 ERROR GENERATION

Any word may be programmed to generate one or more errors. Error specifications follow the last data character. Manually the errors are shifted functions on the keyboard. Manchester, bit count, and zero crossing errors require an additional parameter to specify the bit cell or word length prior to ENTER.

### 2.2.4 GAPS (DEAD LINE TIME)

A dead line (gap) may be inserted in the data string. Gaps are specified as integer multiples of one microsecond up to 99 microseconds. Add two microseconds to the measured dead time to calculate the response time per MIL-STD-1553B.

### 2.2.5 PROGRAM CONTROL WORDS

To aid the user in the development of test programs, five program control instructions are provided:

- o GOSUB — Call Test
- o GOTO — Jump to Test
- o PAUSE — Wait until CONT
- o PRINT — Print Decoder Memory
- o STORE — Store Menu Parameters

These control instructions are embedded into the user tests or active block to control the flow of the tests (2.1.8 Active Data Block Menu).

#### 2.2.5.1 GOSUB <label>

This instruction allows the user to call other tests from the active block being executed. When the called test is completed, the program returns and continues executing the instruction after the GOSUB. In this way sequences of transmissions may be chained together. Called blocks may call other blocks, but the stack is limited to four (4) deep.

#### 2.2.5.2 GOTO <label>

This instruction allows test blocks to point (link) to the next test number to be executed. When the test is completed, control is not returned to the active block. Only the memory size limits the number of test blocks which can be used.

#### 2.2.5.3 PAUSE

This instruction allows the user to indefinitely suspend the test until the CONT key is depressed. When the CONT key is depressed, the test will continue from the point where the PAUSE instruction was inserted.

2.2.5.4 PRINT

BC and RT Simulator Modes: When the PRINT command is encountered in the active block, the Model 553A will print the decoder memory to the print device selected cnrough the CONTROL menu. When the unit completes printing, it will process the next command in the active block. Print commands can only be used with variable and step trigger rates. If no data has been received into the decoder buffer memory, the characters FF:NR will be output to the print device (display or remote interface). Following each print, the decoder is cleared and reset.

Monitor Mode: A dummy data word must be entered prior to the PRINT command. When the PRINT command follows a dummy word in the active block, the 553A will monitor the bus until 256 bus words (including gaps) are received or until 4 milliseconds elapses without bus activity. Then the 553A will print the decoder memory. During the printing, bus activity is not monitored. Print commands can only be used with variable and step trigger rates.

2.2.5.5 STORE (SHIFT MENU)

This instruction allows the user to store the menu set-ups as part of the program. When used, an MU, and 25 Hexadecimal characters representing the packed binary menu definition will appear in the active block and a snap shot of all the menu parameters is taken and stored. When the program encounters the MU instruction, the menu parameters are restored to the way they were when the STORE menu was programmed.

2.2.6 SAVED BLOCKS

Blocks of data may be saved and recalled from RAM, or PROM memory. Saved block are identified by a test number, which is assigned when the active block is saved in RAM or when the PROM is programmed. These labelled blocks may be recalled to replace the active block using the "TEST NO." command, or they may be referenced and executed using the GOTO and GOSUB program controls. Blocks are deleted from RAM with the DELETE command followed by the appropriate test number. Blocks are saved in RAM with the SAVE command . Blocks stored in RAM are limited to 12 characters in the test number name.

When a test block is referenced, the Model 553A first searches for the block in its RAM and then in the external PROM. The first occurrence of the specified label is processed. Approximately 13K characters of space is available in RAM, and 2K in EEPROM, for storing ASCII characters used to create multiple test blocks.

NOTE: Test blocks previously stored in EEPROM are not compatible with Revision 6.9 and must be reloaded and resaved.

### 2.2.7 GENERAL CONSIDERATIONS AND LIMITATIONS

Execution is initiated by a RUN command. An execution pointer is intialized to the beginning of the active block. This execution pointer along with the execution stack is used internally to keep track of program order. Assuming "TRIGGER RATE: STEP" was selected in the menu, execution automatically stops when the execution stack is empty and the execution pointer reaches the end of the active block.

Encoder data are words/gaps which are to be transmitted on the bus. Encoder words to be transmitted contiguously must be grouped sequentially together within a block without intervening program control entries. The end of the block or the first non-encoder word following the sequence of words/gaps defines the message content that will be transmitted. In the fast repeat mode, this string of words/gaps will be repeated continuously. All program sequence control commands, such as a GOSUB, will be ignored. A single encoder sequence may be any combination of words and gaps up to a total of 4096 microseconds of bus time.

Blocks consist of encoder words, program control, and menu control words. Blocks may contain up to 2048 characters including delimiters (see Appendix A).

### 2.2.8 RAMP RESET

This command resets all ramp variables to their initial settngs after a run. When switching back to a fixed amplitude output, the ramp reset should be executed. This is accomplished by entering the active block ("ENTER") followed by the "SHIFT" "RESET" key strokes.

## 2.3 REMOTE INTERFACE

Through the remote interfaces (RS-232 and IEEE 488) menu parameters are set using simple menu commands or the packed menu command (MU and 25 ASCII characters representing the packed menu) which, unlike the manually controlled menu, become a part of the active block. These menu controls are not executed until encountered by the execution pointer after a RUN command. This permits blocks which are saved in memory to include menu parameter adjustments.

Most menu controls consist of two or three letters defining the parameter followed by a number to make the selection or define a value. Transmitter fixed amplitude and zero crossing deviation use two numbers. The trap word has 16 characters (0, 1 or X) following the two letter mnemonic. The remote syntax is given in Appendix A. It should be noted that menu parameters are initialized to the zero (0) selection after powering on the unit.

## 3.0 DATA DISPLAY

In all modes, the MIL-STD-1553 data bus activity is monitored and stored in the decoder. Up to 256 1553 bus words, including gaps, may be stored in the decoder. Three bytes are used per word. The first byte stores the sync polarity, gap information, and the errors associated with the word. The other two bytes contain the 16 bits of data from the word or a measurement of the gap length. This information is processed and is displayed in one of several formats either on the CRT or output to the remote interface. If no data is received, the characters "FF:NR" will be displayed or output.

## 3.1 DISPLAY DEVICE SELECTION

In the menu, a device (CRT, RS-232, IEEE 488 or none) is selected as the display device for PRINT commands. At PAUSE and after execution, the display is on the CRT unless disabled in the menu.

## 3.2 DISPLAY FORMAT

Data from the decoder may be displayed in octal or hexadecimal. The format may be Abbrev, Full or Memory Dump. In the Abbreviated and Full formats, each display line starts with the word count of the first word on that line. In the Abbreviated format, the word count is followed by up to three octal words or four hexadecimal words. Short gaps (less than 32 microseconds) are indicated by two asterisks (**) and long gaps by four asterisks (****). An error associated with a word is indicated by an inverse video single letter suffix (see Table 3.1). The error with the highest precedence is the one which is displayed. For example, if a word had a short word, Manchester, and parity error, it would indicate only the short (S) error in Abbreviated format.

The Full format displays the word count and one word per line along with all of the errors. A time measurement of short gaps is displayed in decimal to within one eighth of a microsecond. That is, the number to the right of the decimal point represents eighths of a microsecond. This gap time is a measurement of the actual dead line.

The memory dump is a 3 byte (6 character per line) hexadecimal display of the decoder status and data bytes. The meaning of the status word bits is shown in Table 3.2. If the status word indicates a short gap, then the third byte is indeterminate and the second byte is the uncorrected gap time. If a log gap is indicated, both the second and third bytes are indeterminate. The uncorrected gap time is in hexadecimal eights of a microsecond and may be corrected to the actual dead line time by converting to decimal and subtracting 21 and dividing by 8.

OC4567 = Command word with data
016567 = Short gap of 10 usec
1898A8 = Data word with a parity error

TABLE 3.1. SPECIAL DISPLAY CHARACTERS

| CHARACTER | DEFINITION | DISPLAY PRECEDENCE |
|---|---|---|
| K | Command Sync | Always |
| L | Long Word Error | 1 |
| S | Short Word Error | 2 |
| M | Manchester Error | 3 |
| P | Parity Error | 4 |
| ** | Short Gap | Abbreviated Format |
| ***** | Long Gap | Abbreviated Format |
| *xx.x | Measured Gap | Full Format Only |

TABLE 3.2. MEMORY DUMP STATUS BYTE

| BIT | DEFINITION(1) |
|---|---|
| 7 | Long Word Error |
| 6 | Short Word Error |
| 5 | Manchester Error |
| 4 | Parity Error |
| 3 | Data |
| 2 | Command Sync |
| 1 | Long Gap |
| 0 | Short Gap |

(1) For each item, the bit set (=1) means the condition is true.

For example:

Memory dump display prints out:

XY $D_1D_2D_3D_4$ (Hexidecimal)

| $X_{HEX}$ | $X_7$ | $X_6$ | $X_5$ | $X_4$ | $Y_{HEX}$ = | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 1 | 01 = Short Gap |
| | 0 | 0 | 0 | 0 | | 0 | 0 | 1 | 1 | 03 = Long Gap |
| | 0 | 0 | 0 | 0 | | 1 | 1 | 0 | 0 | 0C = Command Sync Word |
| | 0 | 0 | 0 | 0 | | 1 | 0 | 0 | 0 | 08 = Data Word |
| | 0 | 0 | 0 | 1 | | 1 | 0 | 0 | 0 | 18 = Data Word w/Parity Error |
| | 0 | 0 | 1 | 0 | | 1 | 0 | 0 | 0 | 28 = Data Word w/Manchester Error |
| | 0 | 1 | 0 | 1 | | 1 | 0 | 0 | 0 | 58 = Short Word w/Parity Error |
| | 1 | 0 | 0 | 0 | | 1 | 0 | 0 | 0 | 88 = Long Word Error |
| | 1 | 1 | 1 | 1 | | 1 | 1 | 1 | 1 | FF = No Decoder Data for Print SRQ ETC. |

## 4.0 REAR PANEL SIGNALS

All signals to/from the Model 553 are available at the rear panel, see Figure 4.1. A description of each of the signals is provided in the following subparagraphs.

### 4.1 MIL-STD-1553 BUS CONNECTORS

Two Trompeter type BJ77 connectors are provided for interface to the MIL-STD-1553 data buses. The center connection is positive. The encoder and decoder are independently switchable between these two connectors. Bus selection is through the menu.

### 4.2 TRANSMITTER SYNC OUTPUT

This TTL level signal provides a low signal while the encoder is active. Applications for this signal include triggering an oscilloscope and gating a noise generator.

### 4.3 TRAP DETECT OUTPUT

This signal is a TTL active low pulse occurring after a word was received with characteristics matching the trap word in the menu.

### 4.4 EXTERNAL TRIGGER INPUT

In the bus controller and RT simulator mode, when external trigger is selected from the menu, a negative going TTL edge at this input causes the data in the encoder to be transmitted.

### 4.5 PROM/EEPROM SOCKET

A 2716 or 2732 PROM preprogrammed with block data may be inserted into this zero insertion force socket. Up to a total of 4,096 characters of user test procedures may be stored in these PROMs.

### 4.6 RS-232C

The RS-232 baud rate is set by switch position as shown in Table 4.1. The standard 25 pin female RS-232 connector is wired as the data set in accordance with the EIA RS-232C standard as shown in Table 4.2. In order to provide proper handshaking, the following signals must be connected as indicated.

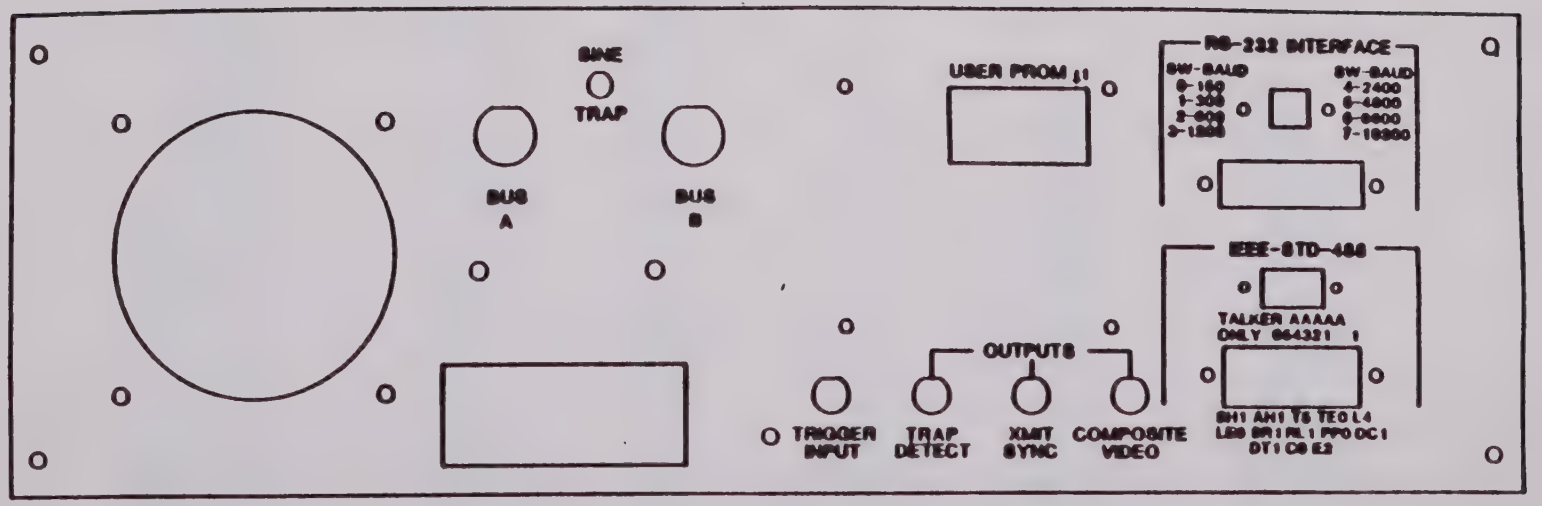



FIGURE 4.1. MODEL 553A REAR PANEL CONNECTORS

TABLE 4.1. RS-232 BAUD RATE SETTINGS

| SWITCH | BAUD RATE |
|---|---|
| 0 | 150 |
| 1 | 300 |
| 2 | 600 |
| 3 | 1200 |
| 4 | 2400 |
| 5 | 4800 |
| 6 | 9600 |
| 7 | 19200 |

TABLE 4.2. RS-232 PIN CONNECTIONS

| FUNCTION | PIN # | MODEL 553 INPUT/OUTPUT |
|---|---|---|
| Received Data (RXD) | 3 | Output |
| Data Set Ready (DSR) | 6 | Output |
| Clear to Send (CTS) | 5 | Output |
| Transmit Data (TXD) | 2 | Input |
| Data Terminal Ready (DTR) | 20 | Input |
| Request to Send (RTS) | 4 | Input |
| Signal Ground | 7 | Common |
| Protective Ground | 1 | Common |

### 4.6.1 CLEAR TO SEND (CTS)

The controller of the Model 553 must monitor this signal and send data only when it is active. Data may be lost otherwise.

### 4.6.2 DATA SET READY (DSR)

This signal is always active when the Model 553 is powered on.

### 4.6.3 REQUEST TO SEND (RTS)

This signal is monitored by the Model 553 to indicate whether a controller or printer is connected. When DTR is inactive, active block commands which would pass data over the RS-232 interface are skipped (e.g. a PRINT command would not be executed, but the active block would proceed with the next instruction). RTS may be made active by a jumper inside the cable to DSR or ground.

### 4.6.4 DATA TERMINAL READY (DTR)

When the controller or printer is capable of receiving data from the Model 553, this signal should be made active. The Model 553 will wait for DTR to go active before passing data and thus will appear to lock up if improperly implemented. If data can be received at any time at the set baud rate, DTR may be made continuously active by tying it to ground.

### 4.6.5 "RT READY" HANDSHAKE

When operating in the RT Simulator mode under RS-232C remote control, the Model 553A signals the controller that it is ready to respond to a command over the 1553 bus by sending the character "T" followed by a carriage return (CR) and line feed (lf). This may be used for handshaking to ensure the 1553 A/B bus controller does not send the command prior to the Model 553 completing its processing and being ready to respond.

## 4.7 IEEE 488

Electrical connection to the Model 553 is through an industry standard IEEE 488 connector located on the rear panel. Device address selection and talk only switch is provided by a six position dip rocker switch located immediately above the IEEE 488 connector. The ON(1) position is at the top of the switch and the OFF(0) at the bottom. Switch address setting "21" is invalid. Please note that these switches are only read and processed at power-on, receipt of device clear (DCL or SDC), or interface clear (IFC). The modes supported by the Model 553 for the IEEE 488 interface are given in Table 4.3.

For End of String (EOS), the Model 553 sends an EOI along with the last character of an output string. A string may be a complete listing of the decoder memory (print command), a comment, an error code (Rxx) or readback functions (Menu, Test Block or Directory). An EOI with data being input to the Model 553 has no significance. If a readback command is not serviced by the host, the Model 553 will still process the next valid command sent to it.

TABLE 4.3. IEEE 488 SUPPORTED MODES

| SUBSET | DESCRIPTION |
|---|---|
| SH1 | Full source handshake ability for use with talk. |
| AH1 | Full acceptor handshake to receive commands and programming information. |
| T5 | "Talk Only" provision. Includes serial poll. |
| TE0 | No secondary talker. |
| L4 | Listen ability. Unlistens if own MTA occurs. No "Listen Only" provision. |
| LE0 | No secondary listener. |
| SR1 | Service request capability. |
| RL1 | Go to local capability. Local lockout command also. |
| PP0 | No parallel poll. |
| DC1 | Device clear capabilities. |
| DT1 | GET. |
| C0 | No controller capability. |
| E2 | Tri-state drivers. |

### 4.7.1 IEEE 488 FUNCTIONS

The following signals are processed as described, by the Model 553.

Device Clear: Device Clear (DCL) and Selective Device Clear (SDC) have the same effect as issuing a "stop" command. If the box is running, it will stop, and the internal pointers will be set to the beginning of the active block. At this time, the active block can be cleared and a new test number loaded.

Group Execute Trigger (GET): The GET function has the same effect as pressing the RUN switch or sending "GO" over a remote interface.

Remote/Local: Except for the SHIFT (LOCAL) key, the keyboard is disabled by a Local Lock Out (LLO) function. The keyboard may be enabled by asserting the Go To Local (GTL) function or by pressing the SHIFT (LOCAL) key. The effect of the LLO and GTL functions is the same as the menu controls LK1 and LK0 (given in Appendix A) respectively, though the two should not be intermixed.

Interface Clear (IFC): The IFC function clears and initializes only the IEEE 488 interface functions. Device Address and Talk Only switches are read by the CPU as part of initialization.

Serial Poll: The controller can determine the state of the Model 553 by reading the status byte (STB function). However, it may be desirable for the Model 553 to interrupt the controller when it needs service. This is possible using the Service Request (SRQ) function. Upon receiving the SRQ, the controller must then read the Status Byte (STB) of all devices until it finds one with the Request for Service (RQS) bit set (bit 6 of the status byte) and then it can perform the required service. The Serial Poll Enable (SPE) and Serial Poll Disable (SPD) are used for this purpose. The Model 553 issues an SRQ as a function of its state and the service request control set by menu commands LS0 through LS6 (details are in Appendix A).

| Remote Command | Function |
|---|---|
| LS0 | No SRQ, clears LS1 through LS6 |
| LS1 | SRQ on print |
| LS2 | SRQ on error |
| LS3 | SRQ on completion of test |
| LS4 | SRQ on pause |
| LS5 | SRQ on RT ready |
| LS6 | SRQ on all of above except LS0 |

These controls are combined and stay set until cleared by LS0 (i.e., LS1 LS3 causes an SRQ on either a print or completion of test). Upon receiving the SRQ and polling to find that the SRQ was from the Model 553, the controller should read the state from the status byte and perform the required service.

Status Byte (STB): The status byte (STB) is sent in response to a serial poll. The bits of STB are defined as follows:

| Bit | |
|---|---|
| 0<br>1<br>2 | Operating State where 0 = Input, 1 = Menu, 2 = Run,<br>3 = Stop, 4 = Pause, 5 = RT Ready, 6 = Ready to Print |
| 3 | Spare |
| 4 | Error: 0 = No, 1 = Yes |
| 5 | Spare |
| 6 | Request for Service (RQS). This device caused the Service Request (SRQ) if set (1). |
| 7 | Spare |

SRQ Interrupt Status:

| Hex | Dec | |
|---|---|---|
| 43 | 67 | SRQ on stop |
| 44 | 68 | SRQ on pause |
| 45 | 69 | SRQ on RT ready |
| 46 | 70 | SRQ on print |
| 50 | 80 | SRQ on input error |
| 53 | 83 | SRQ on execution error |
| 55 | 85 | SRQ on RT not ready |
| 56 | 86 | SRQ on error (print SRQ but no error SRQ) |

SRQ on Non-interrupt Status:

| Hex | Dec | |
|---|---|---|
| 01 | 1 | Menu state |
| 02 | 2 | Run state |
| 03 | 3 | Stop state, no stop SRQ (LS3) |
| 04 | 4 | Pause state, no pause SRQ (LS4) |
| 05 | 5 | RT ready state, no RT ready SRQ (LS5) |
| 06 | 6 | Print state, no print SRQ (LS1) |
| 07 | 7 | None of the above |
| 10 | 16 | Input error, no error SRQ (LS2) |
| 13 | 19 | Execution error, no error or print SRQ (LS1 or LS2) |
| 15 | 21 | RT not ready, no RT ready SRQ (LS5) |

Talk Only (Direct Transfer without a Controller): This mode can be used to print out captured messages locally to an IEEE 488 printer, without a controller. For this function, the printer address must be selected to "31", and the Model 553A TALK ONLY switch set before power-up. A print command must then be used as part of the active block test scenario, and the print device selected as IEEE.

Print Timeout: The Model 553A may need additional time to set up the print out-put string prior to the host controller reading the print request. If a timeout occurs, place a wait statement prior to the read as follows:

```
     SERP = SPOLL(@553A)
     IF SERP = 70 THEN GOTO READ
READ WAIT .1
     ENTER @553A;D$
```

## 4.8 COMPOSITE VIDEO

For displaying the contents of the CRT on a video monitor or video printer, a composite video BNC is located on the rear panel.

SYSTEM CHECKSUM: The 16 bit modulo sum of data is PROM locations 0000H to 3FFFH is displayed for user verification. If the checksum does not match previous values, there has been a change in PROM data.

USER CHECKSUM: The 16 bit modulo sum of data in user PROM locations 4000H to 4FFFH is displayed for user verification. This test is valid only for a 2732 in the user socket. An empty socket or 2716 will give varying checksums because the CPU is then reading from an open circuit.

## 5.2 ENCODER TESTS

Six distinct encoder subtests are executed as follows:

E00-RAM: A memory test similar to CPU RAM test (C00) is run for the encoder memory locations 7400H to 77FFH.

E01-ENCODER POWER UP: After a power on clear, the encoder should be stopped. The STOPL bits of the encoder Status Buffer is verified to be set.

E02-ENCODER START: Two words are transmitted by the encoder. It is verified that the STOPL bit in the Status Buffer is not set while transmitting.

E03-ENCODER STOP AFTER RUN SEQUENCE: The transmitted sequence is verified to have stopped and set the STOPL bit in the Status Buffer.

E04-BASIC ENCODING: A data word followed by an 8 microsecond gap followed by a data word are transmitted and received. It is verified that the word status of the first received word contains no errors, has a data sync and does not indicate a gap. The first byte of data is also verified to be "A8".

E05-GAP ENCODING: The second received word of test E04 is verified to indicate a gap in the word status.

E06-ENCODED WORD FOLLOWS GAP: The word following the gap is verified to have no errors, a data sync and no gap indication. The second byte of data is verified to be "CD".

## 5.3 DECODER TESTS

There are 32 distinct subtests executed as part of the decoder test:

D00-REGISTER CLEAR: The decoder is cleared and the address count and status are read and compared with zero. Failure occurs when they are not all zero.

D01-RAM: A memory test similar to the CPU RAM test (C00) is run for the decoder memory locations 7800H to 7BFFH.

D02-TRAP RAM: Various data are written to and read back from the trap memory 7C00H to 7C17H. Only the two least significant bits of data are used and verified.

D03-BASIC RECEIVE-ADDRESS COUNT: A single data word (5CA3) is transmitted by the encoder and received by the decoder. This test verifies that a word was received by checking to be sure the decoder address count is non-zero.

D04-RECEIVED DATA: The data received in test D03 is compared with 5CA3.

D05-ERRORS: The word received in test D03 is verified to have no errors.

D06-DATA SYNC: The word received in test D03 is verified to have a data sync.

D07-NO GAP: The word received in test D03 is verified to have neither the gap nor long gap flags set in the word status byte.

D08-RECEIVED DATA: Words with various data are transmitted by the encoder and received by the decoder. Received data is compared with transmitted data to verify all states of the data register.

D09-COMMAND SYNC: A word with a command sync is transmitted and received. The word sync bit in the word status of the received word is verified to be a one, indicating a command sync.

D10-PARITY ERROR-FLAG: A word with a parity error is transmitted and received. The word status is verified to have the parity error bit set.

D11-PARITY ERROR-TRAP: Prior to test D10, the trap circuit was set up to trap on an error. This test verifies that the decoder did trap on the parity error by confirming that the TRAP bit is set in the decoder status word.

D12-MANCHESTER ERROR-FLAG: A word with a Manchester error is transmitted and received. The word status is verified to have the Manchester error bit set.

D13-MANCHESTER ERROR-TRAP: Prior to test D12, the trap circuit was set up to trap on an error. This test verifies that the decoder did trap on the Manchester error by confirming that the trap bit is set in the decoder status.

D14-LONG WORD ERROR FLAG (FOLLOWED BY WORD): A long word (21 usec.) followed by a normal word is transmitted and received. The word status of the first word is verified to have the long word error bit set.

D15-LONG WORD ERROR FLAG (FOLLOWED BY GAP): A long word (21 usec.) followed by a 4 usec. gap followed by a normal word is transmitted and received. The word status of the first word is verified to have the long word error bit set.

D16-LONG WORD ERROR TRAP: Prior to test D15, the trap circuit was set up to trap on an error. This test verifies that the decoder did trap on the long word error by confirming that the TRAP bit is set in the decoder status.

D17-SHORT WORD ERROR FLAG (FOLLOWED BY WORD): A short word (19 usec.) followed by a normal word is transmitted and received. The status of the first word is verified to have the short word error bit set.

D18-SHORT WORD ERROR FLAG (FOLLOWED BY GAP): A short word (19 usec.) followed by a 4 usec. gap followed by a normal word is transmitted and received. The status of the first word is verified to have the short word error bit set.

D19-SHORT WORD ERROR TRAP: Prior to test D18, the trap circuit was set up to trap on an error. This test verifies that the decoder did trap on the short word error by confirming that the TRAP bit is set in the decoder status.

D20-SHORT GAP FLAGS: A normal word followed by a 4 usec. gap followed by another normal word is transmitted and received. It is verified that the word status for the gap indicates a gap and not a long gap.

D21-LONG GAP FLAG: A normal word followed by a 32 usec. gap followed by another normal word is transmitted and received. The word status of the gap is verified to indicate a long gap.

D22-GAP TIME: A normal word followed by a gap followed by another normal word is transmitted and received. This test is repeated using various gap times in order to exercise the gap timer circuitry. The received gap time is verified to be within a 1 usec. window of the expected gap time. The encoded gap time in microseconds is displayed in test register R0 while the decoded gap time (corrected) is displayed in R1. The decoded gap time is measured in eighths of microseconds and is corrected by subtracting 8 from the sync of the following word. Compare R0 and R1 by shifting R0 three bits to the left.

D23-TRAP COUNT: The decoder is set up to trap on an error. Several words with interlaced gaps are transmitted and received followed by a word with a parity error followed by a normal word. The trap address count is verified to be correct.

D24-ADDRESS COUNT: After test D23, the address count is verified to be correct.

D25-ADDRESS COUNT OVERFLOW NOT SET: After test D24, the address overflow in decoder status register, is verified not to be set.

D26-ADDRESS COUNT OVERFLOW SET: A sequence as in test D23 with N=129 is transmitted and received. The address overflow in decoder status register, is verified to be set.

D27-TRAP AT END OF DATA: The decoder is set up to trap on an error and for the trap word to be at the end of data (i.e. no more words received after the trap). A word with a parity error followed by two normal words separated by gaps is transmitted and received. The address count is verified to be equal to 2 and the trap complete bit in the decoder status is verified to be set.

D28-TRAP AT MIDDLE OF DATA: The decoder is set up to trap on an error and for the trap word to be at the middle of data (i.e. up to 127 words may follow the trap). A word with a parity error followed by 140 decoder words are transmitted and received. It is verified that the address count = 128 indicating that the decoder stopped receiving 127 words after the trap.

D29-TRAP AT BEGINNING OF DATA: The decoder is set up to trap on an error and for the trap word to be at the beginning of the data (i.e. up to 255 words may follow the trap). A word with a parity error followed by 260 decoder words are transmitted and received. It is verified that the address count = 0 indicating that the decoder stopped receiving 255 words after the trap.

D30-TRAP DATA COMPARE: The decoder is set up to trap on data 0101 XXXX XXXX 1100. Words DA3C, 1A3C, 5A3C and AA33 are transmitted and received. It is verified that the trap address count = 3 indicating that it trapped on the 5A3C.

D31-TRAP ON COMMAND SYNC: The decoder is set up to trap on a command sync. A data word, command word and data word are transmitted and received. It is verified that the trap address count = 2 indicating that it trapped on the command word.

D32-TRAP ON DATA SYNC: The decoder is set up to trap on a data sync. Two command words, a data word and a command word are transmitted and received. The trap address count is verified to equal 3 indicating the trap on the data word.

## 6.0 INSTALLATION AND MAINTENANCE

### 6.1 UNPACKING AND INSPECTION

The Model 553 is packed in a molded, plastic foam form, within a cardboard carton. The molded form holds the unit securely in the carton and absorbs any reasonable external shock, normally encountered in transit. Carefully remove the unit from the carton and inspect the exterior of the instrument for any signs of damage.

The shipping container and packing material should be retained, in case reshipment is required.

Included in the shipping container with the instrument are the instruction manual, power cord and external option accessories.

### 6.2 MECHANICAL INSTALLATION

The Model 553 is equipped with a collapsible tilt bail, which may be used to elevate the front of the instrument for convenient bench use.

### 6.3 ELECTRICAL INSTALLATION

Prior to connecting power to the Model 553, confirm that the primary power source is compatible with the unit's source requirements. The Model 553 is fitted with a combined AC connector, fuse holder and voltage selector, on the rear panel. This enables the unit to be operated from the following power sources:

a) 90-132 VAC, 2 amp fuse.
b) 180-264 VAC, 1 amp fuse.

In order to select a different operating voltage, the following procedure should be adopted:

a) Remove AC power cord.

b) Slide connector window over to cover AC receptacle.

c) Remove fuse by lifting fuse release lever.

d) Remove printed circuit board selector.

e) Reorientate and install selector board, such that desired voltage will be visible upon reassembly.

f) Return fuse release lever to original position and install fuse of correct rating.

g) Slide window over, to cover fuse, and check that desired operating voltage is now visible.

h) Make certain that power switch is in the OFF (lower half of switch depressed) position and install power cord.

An AC line cord, having a three-pin plug is supplied with the instrument. When the cord is plugged into the Model 553's rear panel receptacle, the round pin of the plug is connected to the instrument's chassis. This pin must be connected to a good quality earth ground when the plug is installed in the user's primary power receptacle.

Note: Chassis ground and logic ground are internally connected.

## 6.4 FUNCTIONAL VERIFICATION

The purpose of this section is to provide calibration or metrology lab personnel with a means of verifying the correct operation of the Model 553. The procedure should be undertaken at the periodic maintenance interval.

There are two tests and two calibrations which may be performed:

1) Self Test
2) Bus Coupling Test
3) Transmitter Amplitude Calibration
4) Zero-crossing Calibration

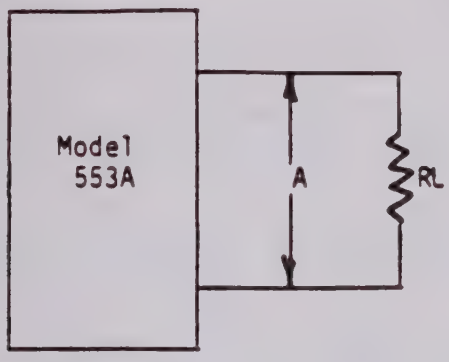
### 6.4.1 SELF TEST

Self Test is performed each time the unit is powered-on and is described in Section 5 of this manual.

## 6.4.2 BUS COUPLING TEST

This test checks that the relays, transformers, and resistive loads are present to ensure the correct signal levels for the different bus coupling options.

Set-up: The figure below shows the Model 553A as a bus terminal, with a load specified by MIL-STD-1553B. The value of this load changes for the Direct Coupled test and the Transformer Coupled test.




Oscilloscope Connection:

a) Place channel 1 of the oscilloscoe at point A1. This will be connected to the center conductor of either "BUS A" or "BUS B" located on the rear panel of the Model 553A.

b) Place channel 2 of the oscilloscoe at point A2. This will be connected to the next outer conductor of the same connector as in step a.

c) Connect the oscilloscope ground to the outer shield of the connector.

d) Invert channel 2.

e) Add channel 1 to channel 2.

f) Set the scale to 10V per division.

g) Connect the trigger input of the scope to the "XMIT SYNC" BNC connector on the Model 553A rear panel.

Test Sequence: DIRECT COUPLED STUBS

a) For this test, the load termination must be equal to 35 ohms ± 2%.

b) Using "BUS A" of the Model 553A, hook up an oscilloscope as in the above procedure.

c) In the Model 553A menus, set the mode to "BC SIMULATOR".

d) In the Model 553A menus, set the following:

| | |
|---|---|
| SIMULATE BUS: | NO |
| BUS COUPLING: | DIRECT |
| PROTOCOL: | 1553B |

e) In the Model 553A menus, set the TRANSMITTER to "BUS A" and the RECEIVER to "BUS A".

f) In the Model 553A menus, set the TRIGGER RATE to "FAST".

g) Enter the data pattern "5A5A" in the Active Block using the key sequency (ENTER,5,A,5,A,ENTER).

h) Run the instrument and verify that the output is within the range of 6.0 to 9.0 volts, peak-to-peak, when measured between points A1 and A2. Stop the instrument.

Test Sequence: TRANSFORMER COUPLED STUBS

a) For this test, the load termination must be equal to 70 ohms +/- 2%.

b) Using "BUS A" of the Model 553A, hook up an oscilloscope as in the above listed procedure.

c) In the Model 553A menus, set the mode to "BC SIMULATOR".

d) In the Model 553A menus, set the following:

| | |
|---|---|
| SIMULATE BUS: | NO |
| BUS COUPLING: | XFMR |
| PROTOCOL: | 1553B |

e) In the Model 553A menus, set the TRANSMITTER to "BUS A" and the RECEIVER to "BUS A".

f) In the Model 553A menus, set the TRIGGER RATE to "FAST".

g) Enter the data pattern "5A5A" in the Active Block using the key sequence (ENTER,5,A,5,A,ENTER).

h) Run the instrument and verify that the output is within the range of 18.0 to 27.0 volts, peak-to-peak, when measured between points A1 and A2. Stop the instrument.

Test Sequence: Repeat the above tests for "BUS B" and for the Sinusoidal signal outputs, if installed. Be sure to select "BUS B" in the Model 553A menus.

### 6.4.3 TRANSMITTER AMPLITUDE CALIBRATION

Remove the Model 553A top cover. The upper most CCA is the Encoder CCA. Connect a DC voltmeter to "TP2" on the Encoder CCA. With the Model 553A power on, adjust "R18" for 15 +/-0.5 volts. Turning R18 clockwise will decrease the voltage.

### 6.4.4 ZERO CROSSING DEVIATION TEST

This test is used to verify that the zero crossing deviation circuitry is functioning properly, and is adjusted within calibration specifications. For the Zero Crossing Deviation Test, perform the following procedure:

1) Connect scope probe channel 1 to Bus A center conductor on the rear panel of the Model 553A.

2) Connect scope probe channel 2 to XMIT SYNC on the rear panel. Trigger oscilloscope on channel 2 negative slope.

3) Enter "0000" in the active block of the Model 553A; change the trigger rate to fast repeat. All other parameters remain the same.

4) Run the instrument. Set the scope the delayed sweep at 50ns/div and adjust the scope delay so that bit time (figure 1) is centered on the screen as shown in figure 2.

5) Stop the instrument and change the contents of the active block to "0000RZ5".

6) Run the instrument. Bit time 5 should remain centered on the screen. If bit time 5 has moved more than ±6ns, the unit is out of calibration. If this portion passes then continue.

7) Stop the instrument. On the transmit zero crossing menu, change the fixed deviation to -249ns.

8) Run the instrument. Bit time 5 should have deviated -249ns ±6ns as in figure 3. If bit time 5 has deviated out of tolerance then the unit is out of calibration, and must be serviced by the factory.

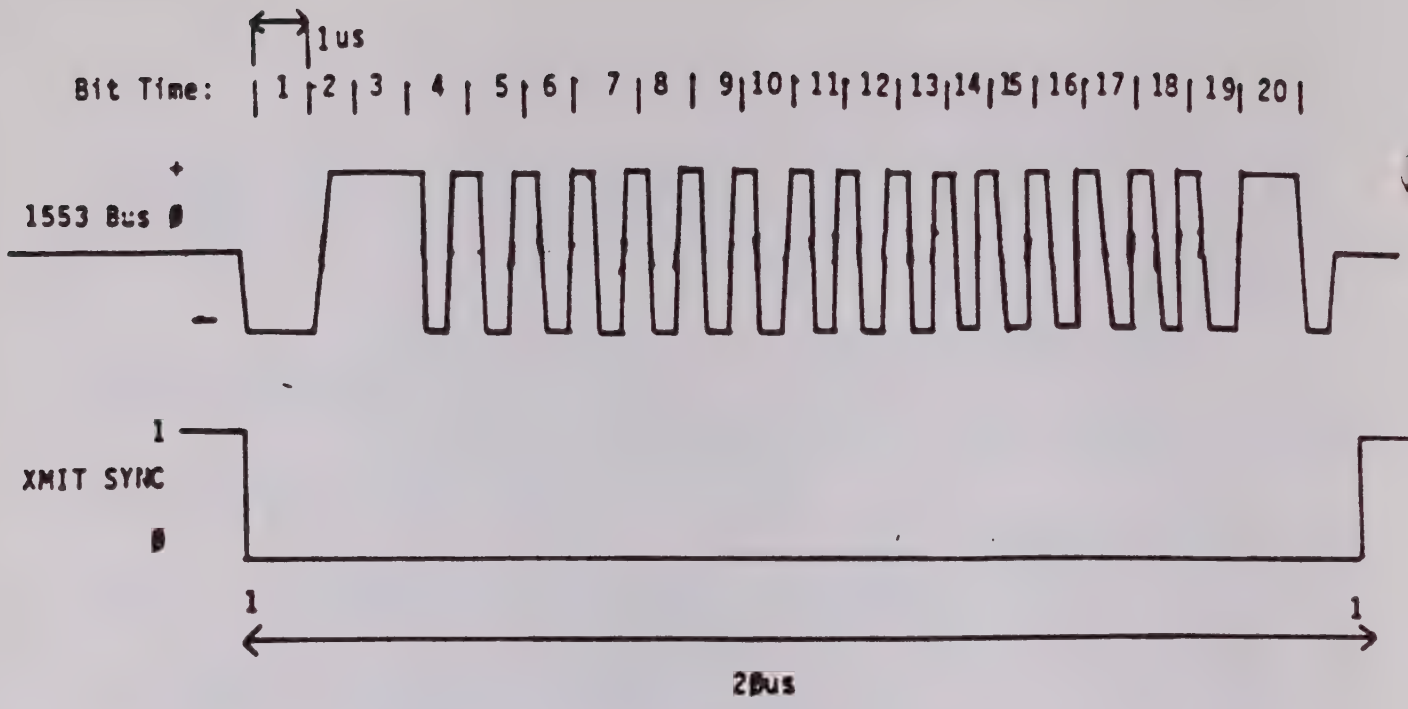



Figure 6-1

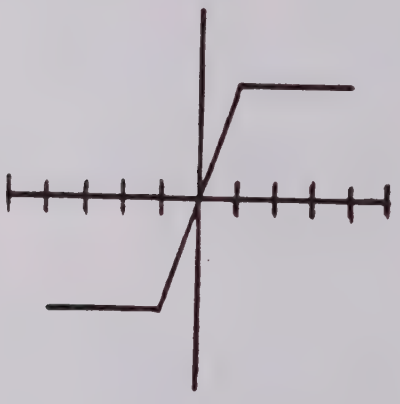



Figure 6-2

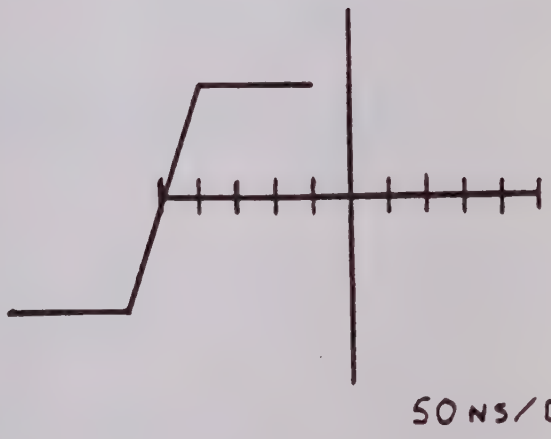



Figure 6-3

# APPENDIX A. PROGRAMMING SYNTAX

## A.1. NOTATION

( ) = required parameter; multiple items mean one (1) entry must be present.

[ ] = optional parameter; multiple items mean one (1) entry may be present.

ascii = Any ASCII character except $ and @.
bit time = Decimal number in range to 20.
c = Character in range 0 to 9, or A to Z.
cntrl c = "ETX" in ASCII (03H) functions as the "STOP" command.
NOTE: Should not be sent with other commands.
d = Digit in range 0 to 9 (decimal).
delimiter = Space (20H), comma (2CH), carriage return (0DH) or line feed (0AH). Note: In PROM, the only valid delimiter is a space.
device = (0 = CRT, 1 = IEEE 488, 2 = RS-232).
K = Command sync (default is data sync).
n = Digit in range 0 to 9, or A to F (hexadecimal).
space = 20H.
t = Character 0, 1 or X.
W = Trap word = ttttttttttttttt.
@ = 40H.
$ = 24H.

## A.2. PROGRAMMING SYNTAX

Programming the Model 553A over a remote interface involves sending a character (ASCII) stream to Model 553A in either single or multiple transfers. The character (ASCII) set utilized by the Model 553A is upper case and given in Table A.1. Essentially there are two (2) types of commands, BLOCK commands and RUNTIME commands. BLOCK commands are processed and saved in the active (current) block but are not executed until a GO command is received. RUNTIME commands are processed and executed immediately. If a syntax error is detected during processing, the character "R" followed by the error number as given in Appendix D is transmitted over the remote interface.

## TABLE A.1. ASCII CHARACTER CODES

| BITS 4 to 6 | -- | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|---|
| BITS 0 TO 3 | 0 | NUL | DLE | SP | 0 | @ | P | ` | p |
| | 1 | SOH | DC1 | ! | 1 | A | Q | a | q |
| | 2 | STX | DC2 | " | 2 | B | R | b | r |
| | 3 | ETX | DC3 | # | 3 | C | S | c | s |
| | 4 | EOT | DC4 | $ | 4 | D | T | d | t |
| | 5 | ENQ | NAK | % | 5 | E | U | e | u |
| | 6 | ACK | SYN | & | 6 | F | V | f | v |
| | 7 | BEL | ETB | ' | 7 | G | W | g | w |
| | 8 | BS | CAN | ( | 8 | H | X | h | x |
| | 9 | HT | EM | ) | 9 | I | Y | i | y |
| | A | LF | SUB | * | : | J | Z | j | z |
| | B | VT | ESC | + | ; | K | [ | k | { |
| | C | FF | FS | , | < | L | \ | l | \| |
| | D | CR | GS | - | = | M | ] | m | } |
| | E | SO | RS | . | > | N | ^ | n | ~ |
| | F | SI | US | / | ? | O | _ | o | DEL |

## A.2.1 BLOCK COMMANDS

Individual BLOCK commands must be separated by delimiters and may be any of the following: 1553_WORD, GAP, PROGRAM_CONTROL, or MENU_CONTROL.

a) 1553_WORD = [K](nnnn) [(RP) / (RM)(bit time) / (RC)(d)[d] / (RZ)(bit time)] ... [(RP) / (RM)(bit time) / (RC)(d)[d] / (RZ)(bit time)]

where:

K = Generates a Command/Status Sync.

nnnn = Actual data contents to be transmitted.

RP = Parity error.

RM = Manchester error at specified bit time.

RC = Count error where specified bit count will be transmitted.

RZ = Zero crossing deviation will be generated at specified bit time according to current menu settings.

b) GAP = (GP)(d)[d]

c) PROGRAM_CONTROL = (GS)(c) ... [c]
(GT)(c) ... [c]
(PS)
(PR)
($S)(device)(delimiter)(ascii text)($E)

where:

GS = GOSUB to the specified label.

GT = GOTO the specified label.

PS = Pause.

PR = Print.

($S)(device)(delimiter)...($E) = Display (comment) the specified text to the indicated device. The ASCII text cannot contain a "$", and can be a maximum of 27 characters. Device can be one of the following:

0 = CRT
1 = IEEE
2 = 232
3 = None

d) MENU_CONTROL. In the following "x" is variable as indicated and "nn" represents a hexadecimal byte. The given mnemonic is the actual characters to be transmitted to the Model 553A to achieve the desired function.

| Mnemonic | Function |
|---|---|
| MU | Packed Menu: Remote command or shift menu key. When entered in active block, the current menu set up is saved in a packed form and at execution time is unpacked and menu initialized. |
| MUnn...n | Packed Menu: Remote command defining 25 packed menu characters in hexadecimal form, see Appendix B, Example 15. |
| MMx | Mode: 0 = BC Simulator; 1 = RT Simulator; 2 = Monitor; 3 = Self Test |
| MLx | Internal Bus: 0 = Yes; 1 = No |
| MCx | Coupling: 0 = Direct; 1 = Transformer |
| MPx | Protocol: 0 = 1553B; 1 = 1553A |
| TBx | Transmitter Bus: 0 = A; 1 = B |
| TXx | Transmitter Trigger: 0 = Internal; 1 = External |
| TAx | Transmitter Amplitude: 0 = Full; 1 = Adjust; 2 = Set |
| TSnn | Transmitter Fixed Amplitude Setting: % of full amplitude = 0.4% x (nn)<br><br>NOTE: Use TA1 prior to TZnn and use TA2 after. |
| TSRIullt | Ramp Transmitter Amplitude where:<br><br>lu = maximum limit<br><br>ll = minimum limit<br><br>t = ramp type (0-2)<br>0 = CYCLE ON MIN<br>1 = CYCLE ON NR<br>2 = HOLD ON MIN<br>3 = HOLD ON NR<br>4 = STOP ON MIN<br>5 = STOP ON NR |

NOTE: Zero crossing must be set to fixed before selecting ramp transmitter amplitude.

| Mnemonic | Function |
|---|---|
| TCx | Transmitter Fixed Zero Crossing: 0 = Mid bit; 1 = Bit end |
| TDx | Transmitter Zero Crossing Deviation: 0 = Zero; 1 = Adjust; 2 = Set |
| TZnn | Transmitter Zero Crossing Deviation Value: Range ±300 ns.<br><br>Value (in ns.) = (nn - 80H) x 3 for nn > 80H<br>-(80H - nnH) x 3 for nn < 80H<br>0 for nn = 80H<br><br>NOTE: Use TD1 prior to TZnn and use TD2 after. |
| TZR11dt | Ramp Transmitter Zero Crossing where:<br><br>11 = limit<br><br>d = direction (0-2)<br>0 = NEG.<br>1 = POS.<br>2 = POS. & NEG.<br><br>t = ramp type (0-5)<br>0 = CYCLE ON MIN<br>1 = CYCLE ON NR<br>2 = HOLD ON MIN<br>3 = HOLD ON NR<br>4 = STOP ON MIN<br>5 = STOP ON NR<br><br>NOTE: Amplitude must be set to fixed before selecting ramp zero crossing. |
| TMx | Manchester Error Type: 0 = 00 ; 1 = 01 ; 2 = 10 ; 3 = 11 where the binary numbers represent the polarity of the two halves of the bit cell; e.g. "00" implies "0" for first half and "0" for second half. |
| RBx | Receiver Bus: 0 = A; 1 = B |
| RXx | Receive Xmit Data: 0 = Yes; 1 = No |
| VSx | Trap Word Sync: 0 = Command; 1 = Data; 2 = Don't Care |
| VWw | Trap Word Data: w defines 1 to 16 bits as 0, 1 or X (Don't Care)<br><br>NOTE: Only 1, 0, and X are valid characters and 1 to 16 characters may be defined, with undefined bits unchanged. Not valid for VTO (trap on anything). |

VWHnnnn — Trap Word Data: nnnn defines 4 hexadecimal characters where Don't Cares are not allowed.

VPx — Trap Display Position: 0 = Post trigger; 1 = Pre trigger; 2 = Centered. Valid in Monitor mode only.

VTx — Trap On: 0 = Anything; 1 = Trap word only; 2 = Trap word or error; 3 = Error only.

LDx — Display Numbers: 0 = Hexadecimal; 1 = Octal.

LIx — Input Numbers: 0 = Hexadecimal; 1 = Octal.

LPx — Print Device: 0 = CRT; 1 = IEEE 488; 2 = RS-232; 3 = None

LCx — CRT Display: 0 = Enabled; 1 = Disabled. The Model 553A operating speed is increased by eliminating processing associated with formatting and displaying data. When disabled, the CRT will not display the active block nor decoder memory contents, however comments, errors, and operating state are displayed.

LFx — Display Format: 0 = Abbreviated; 1 = Full; 2 = Memory Dump

LKx — Keyboard Disable: 0 = Enabled; 1 = Disabled

LTxnn — Trigger: 0 = Single; 1 = Fast; Repeat (approximately 4 ms wait); 2 = Slow Repeat (nn = 10 ms/count, 10-1000 ms)

NOTE: LT2 sets slow repeat to 1 second.

LSx — IEEE Service Request Controls:

LSx IEEE SERVICE REQUESTSST:

| | |
|---|---|
| LS0 | Clear all SRQ requests |
| LS1 | SRQ on ready to print |
| LS2 | SRQ on detection of error |
| LS3 | SRQ on stop |
| LS4 | SRQ on pause request |
| LS5 | SRQ on RT ready or RT not ready |
| LS6 | Set all SRQ requests |

STx — Self Test: 0 = All; 1 = CPU; 2 = Decoder; 3 = Encoder

## A.2.2 RUNTIME COMMANDS

Individual RUNTIME commands must be separated by delimiters and may be any of the following:

a) SAVE BLOCK: (SV)(c) ... [c] for RAM
(SE)(c) ... [c] for EEPROM

where:

(c) ... [c] is a 1 to 12 character label

SV = Save the current active block as the given label in RAM

SE = Save the current active block as the given label in EEPROM

b) Delete Block: (XN)(c) ... [c]

where:

XN = Delete the previously saved block which has the specified label.

c) Recall a Block: (TN)(c) ... [c]

where:

TN = Recalls a previously saved block, or pre-programmed block, which has the specified label into the current (active) block.

NOTE: Also resets ramp, enables "TSR" or "TZR command.

d) Clear Current (Active) Block: (XA)

where:

XA = Clears the entire contents of the current (active) block.

NOTE: Also resets ramp, enables "TSR" or "TZR" command.

e) Ramp Reset: RS which will reset ramp values and hold flag

f) Ramp Remote Echo: RE[Y/N]

where:

"Y" will output Ramp Value each slow repeat cycle.

NOTE: For IEEE 488, the print SRQ (LS1) must be set.

g) Format EEPROM: FM

where:

EEPROM is initialized to empty.

h) Remote Menu Readback: RM

where:

a new page of the menu is outputted for each request.

i) Remote Block Readback: DSnn ... n[$]

where:

nn ... n = 1 to 12 character label or null for active block.

$ = optional next page flag.

See Appendix B, Example 16.

j) Remote Directory Readback: DR[$]

where:

$ indicates next page of directory display.

See Appendix B, Example 17.

k) Error Readback: ER

where:

If the SRQ on ERror "LS2" is not set, then the "ER" command will give the last error condition encountered.

If the SRQ on Error "LS2" is set, then the "ER" command will give the first error condition encountered.

NOTE: An "*" indicates no error.

l) Run: (GO).

m) Continue: (cntrl r); A "Control R" is the ASCII "DC2" = (12H).

n) Stop: (cntrl c); A "Control C" is the ASCII "ETX" = (03H).

o) Stop & Print: A "Control-D" is the ASCII "EOT" = (044).
The same requirements for a "PR" command apply, including the "SRQ on print enable" and specifying IEEE 488 as the print device.

p) Clear Entry Delete.

where:

delete is the ASCII "DEL" = (7FH).

NOTE: To be used by an RS-232C terminal where a single character is input at a time, not for character string use.

q) Clear RAM Storage: SC.

## A.3 PRE-PROGRAMMING A PROM

A PROM may be pre-programmed and placed in the external PROM socket at the rear panel of the Model 553. The exact same character stream (commands) which are used in remote programming are used to program the PROM(1) along with block header information for each block which is to be recalled to the active block (TN) or referenced in program control (GOSUB or GOTO).

The block header information is "@" label "space" and would appear as:

BLOCK HEADER = (@)((c) ... [c])(space)(commands) ...
(@)((c) ... [c])(space)(commands)(@)(space)

(1) Note: The only delimiter allowed in pre-programmed PROM blocks is the space (20H).

Labelled blocks in PROM are identified by their label header. All characters in PROM are ASCII. The header is a single word beginning with the character "@" followed by the label, followed by a "space" (20H). Labels referenced by GOTO and GOSUB commands may be of any length, but are limited to 23 characters in order to recall or replace the active block. The block words (encoder, menu and program controls) follow the header and are programmed the same as data passed over the automated interfaces except that a "space" (20H) is the only valid delimiter (i.e., no commas or carriage returns). The end of the labelled block is indicated by the start of the next block (@), so the last labelled block in a PROM should be terminated with an "@", "space" (40H, 20H)(see Appendix A). These headers are automatically inserted when the active block is saved in RAM via the SAVE command.

# APPENDIX B. EXAMPLES

Characters in parenthesis represent one manual keystroke. The lower case letter d represents any delimiter (space, comma, carriage return or line feed).

## EXAMPLE 1: Input Normal Data

Manual: (CMD SYNC)(1)(0)(6)(1)(ENTER)(8)(7)(6)(5)(ENTER)

Automated: K1061d8765d

Here the command word 1061H followd by the data word 8765H is entered into the active block and displayed as K1061 8765 on the CRT. Assuming the Model 553 is in the BC mode, pressing RUN, or issuing "GO", causes these two words in the active block to be transmitted as specified by the parameters in the menu. With the Model 553A's receiver on the same bus as the transmitter, the two words are wrapped around through the receiver and displayed along with any response from other units on the bus.

## EXAMPLE 2: Input a Word with an Error

Manual: (CMD SYNC)(1)(4)(2)(3)(SHIFT)(P-ERR)(ENTER)

Automated: K1423RPd

The command word 1423H is entered with a parity error and displayed as K1423RP.

## EXAMPLE 3: Input a Word with Multiple Errors

Manual: (8)(7)(6)(5)(SHIFT)(O-XING)(1)(2)(SHIFT)(M-ERR)(5)(ENTER)

Automated: 8765RZ12RM5d

The data word 8765H is entered with a Manchester error in bit cell 5 and the zero crossing in bit cell 12 will be deviated according to the parameters in the menu. This is displayed as 8765RZ12RM5.

## EXAMPLE 4: Input a Gap

Manual: (SHIFT)(GAP)(4)(ENTER)

Automated: GP4d

A 4 microsecond deadline is inserted and displayed as GP4. When inserted between the words of EXAMPLE 1 (i.e., K1061 GP4 8765), a 4 microsecond dead line is generated between the command word (K1061) and the data word (8765).

EXAMPLE 5: A Block with a Program Control

Automated: K1423dGT27

Upon execution, the command word (K1423H) is transmitted on the bus. There is no pause to display bus activity before Block 27 is executed.

EXAMPLE 6: A Block with a Pause and Program Control

Automated: K1423dPSdGT27

Here the bus activity resulting from the K1423H command word is displayed after a RUN command. Block 27 is then executed when a CONTINUE command is given.

EXAMPLE 7: A Block Exclusively with Program Controls

Active Block: GS5dGS14

Here the active block does not contain any words to be transmitted. Upon execution, the program immediately proceeds to Block 5. When execution of Block 5 is complete, Block 14 is executed.

EXAMPLE 8: Save the Data in the Active Block

Manual: (SHIFT)(SAVE)(2)(8)(ENTER)

Automated: SV28d

EXAMPLE 9: A Cross Talk Test

Pass the following over an automated interface:

XAdTB0dRB1dK1423dPRdRB0dG0

This sequence occurs:

XA - The active block is cleared.

An active block is created with:

TB0 RB1 K1423 PR RB0

GO - The active block is executed:

TB0 - Set transmitter to bus A
RB1 - Set receiver to bus B
K1423 - Load encoder with command word K1423H
PR - Transmit data (K1423H) in encoder and print response
RB0 - Set receiver back to bus A

The resulting printout should show that neither the transmitted data nor a response were received.

EXAMPLE 10: An RT to RT Test with the Unit Under Test as the Transmitting RT

Active Block: K2843dK1443

The first command word instructs the receiving RT, which may or may not actually exist during the test, to receive three words. The unit under test should respond to the second command word with a status word and three data words.

EXAMPLE 11: An RT to RT Test with the Unit Under Test as the Receiving RT

Active Block: K1043dK2C43dGP4dK2800d4321dABCDd6789

The Model 553A provides the two command words, a 4 microsecond deadline time gap and the status and data words of the transmitting RT.

EXAMPLE 12: Abbrev Display Format

Display the bus activity resulting from EXAMPLE 11.

```
000     ****     K1043     K2C43      **
004    K2800      4321      ABCD     6789
```

EXAMPLE 13: Full Display Format

Display the bus activity resulting from EXAMPLE 1 and assume a short word, Manchester and parity error in the responding status word.

```
000    ****
001    K1061
002    8765
003    * 6.0
004    K1000SMP  (status response from second unit)
```

Note that the response time gap was measured as six and seven eights microseconds.

EXAMPLE 14: Memory Dump Display Format

Display a memory dump of the bus activity as in EXAMPLE 13.

```
038C5D
041061
008765
014523
741000
```

EXAMPLE 15: Remote Menu Command

The remote menu command has two formats: MU and MUnn ... n. Use of these two commands and the readback block command (RB) can be used to create a packed menu.

a) Execute XA, clear active block

b) Execute MU, pack current menu set up

c) Execute menu commands to modify initial menu set up

d) Execute DS, readback new packed menu set up

EXAMPLE 16: Readback Active or Test Block

DS will readback first page of active block

DS will readback next page of active block

DSnn ... n will readback first page of block nn ... n

DSnn ... n$ will readback next page of block nn ... n

```
$S BLOCK nnnnnnnnnnnn (TOP)      $E
                                 display position ALL
K0000 1111 2222 3333 4444 5555                    TOP
KAAAA BBBB                                        MIDDLE
                                                  END
```

where:

ALL = indicates all is displayed in one page.

TOP = indicates first page and more is to come.

MIDDLE = indicates not first page and more is to come.

END = not all is displayed but at end of display

EXAMPLE 17: Readback Block Directory

The Directory Readback command (DR) is used for obtaining a list of all test block numbers resident in the internal RAM or external EPROM memory.

RESULTS:

```
$S  BLOCK DIRECTORY   (ALL)  $E

  TEST1, TEST2, TEST3, 44, 55, 66, AA, BBB <EXT> 31, 32, 33
```

EXAMPLE 18: Display with Xmit Data - NO

This selection is useful for suppressing the BC data and only examining the RT responses. It must be used with the variable trigger rate (0-1000 ms), which allows you to analyze responses on a message-by-message basis.

Variable Repeat:

```
K 1111 2222 3333  PR  K 4444 5555  PR  K 6666 7777 8888  PR
```

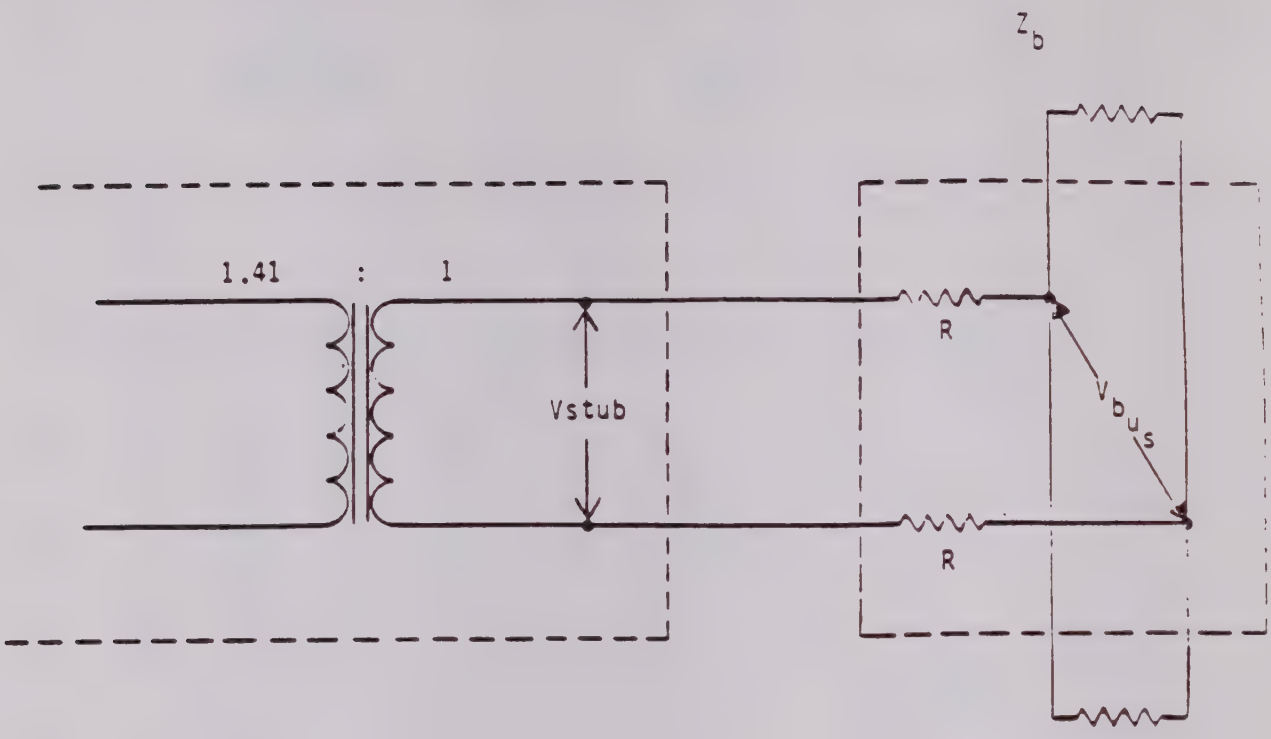
After each BC message is transmitted, the response will be received, a print request generated, and then the next message will be output.

## APPENDIX C. OPTIONS FOR 553A OUTPUT

### MENU SELECTION

| 1553A | 1553B | | |
|---|---|---|---|
| If the following has been selected:<br><br>1. No<br>2. Direct refer to Fig 1A<br>3. 1553A | If the following has been selected:<br><br>1. No<br>2. Direct refer to Fig 1B<br>3. 1553B | Direct | TYPICALLY AN EXTERNAL BUS ENVIRONMENT |
| If the following has been selected:<br><br>1. No<br>2. Xformer refer to Fig 2A<br>3. 1553A | If the following has been selected:<br><br>1. No<br>2. Xformer refer to Fig 2B<br>3. 1553B | Xformer | |
| If the following has been selected:<br><br>1. Yes<br>2. Direct refer to Fig 3A<br>3. 1553A | If the following has been selected:<br><br>1. Yes<br>2. Direct refer to Fig 3B<br>3. 1553B | Direct | TYPICALLY AN LRU OR INSTRUMENT UNDER TEST ENVIRONMENT |
| If the following has been selected:<br><br>1. Yes<br>2. Xformer refer to Fig 4A<br>3. 1553A | If the following has been selected:<br><br>1. Yes<br>2. Xformer refer to Fig 4B<br>3. 1553B | Xformer | |

FIGURE 1A. 1553A DIRECT COUPLED TO A BUS




Model 553A

1553B Bus Coupler

Zb = 70Ω ±10% (spec)
R = .75 x Zb ±5% (spec)

553A to Instrument

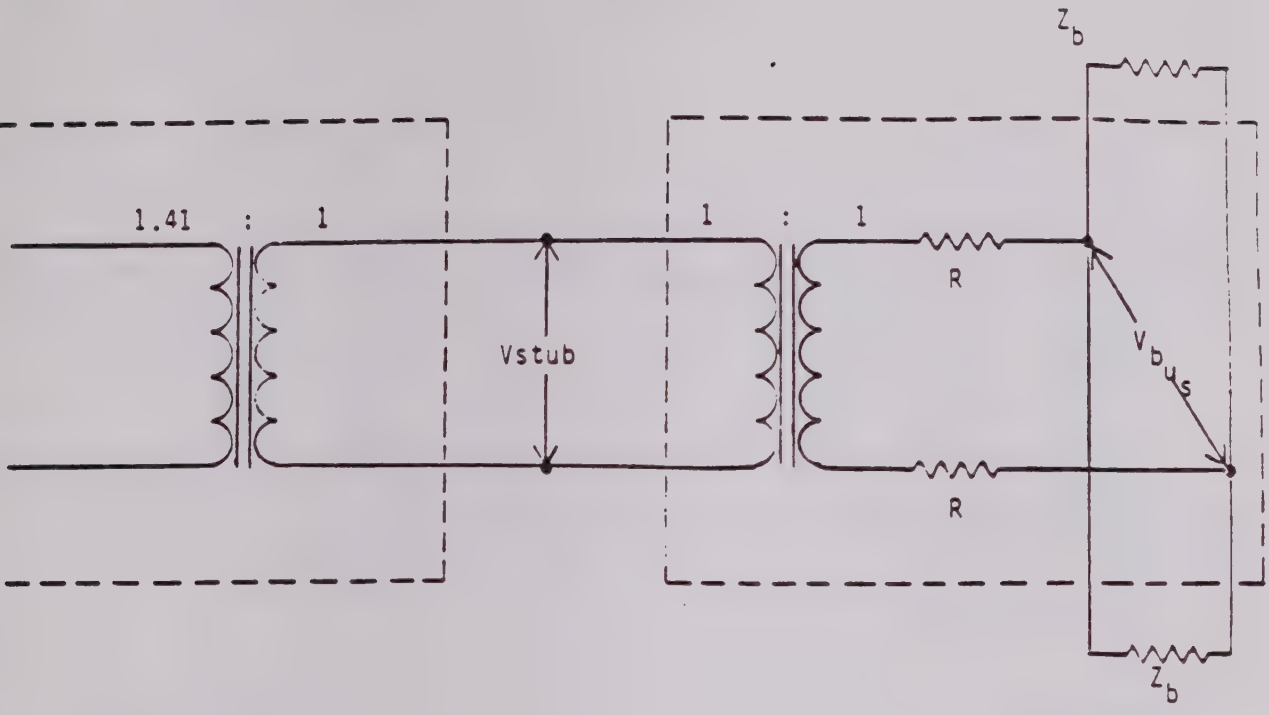
Vstub = 0-27 volts

$$V_{bus} = V_{stub}\left[\frac{Zb/2}{2R+Zb/2}\right]$$

= 0-6.75 volts

$V_{STUB}$ = 16.1V (Typ)
$V_{BUS}$ = 3.6V (Typ)

FIGURE 2A. 1553A TRANSFORMER COUPLED TO A BUS




Model 553A

1553A Bus Coupler

Zb = 70Ω ±10% (spec)
R = .75 x Zb ±5% (spec)

553A to Instrument

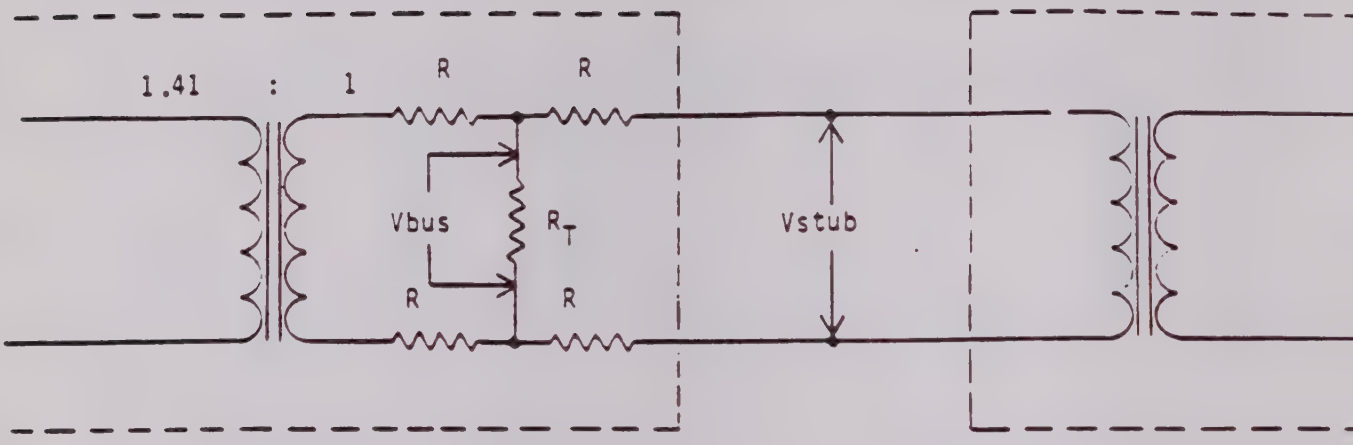
Vstub = 0-27 volts

$$V_{bus} = V_{stub}\left[\frac{Zb/2}{2R+Zb/2}\right]$$

= 0-6.75 volts

$V_{STUB}$ = 16.1V (Typ)
$V_{BUS}$ = 2.5V (Typ)

FIGURE 3A/4A. 1553A COUPLING TO AN INSTRUMENT OR LRU




Model 553A

1553A Instrument

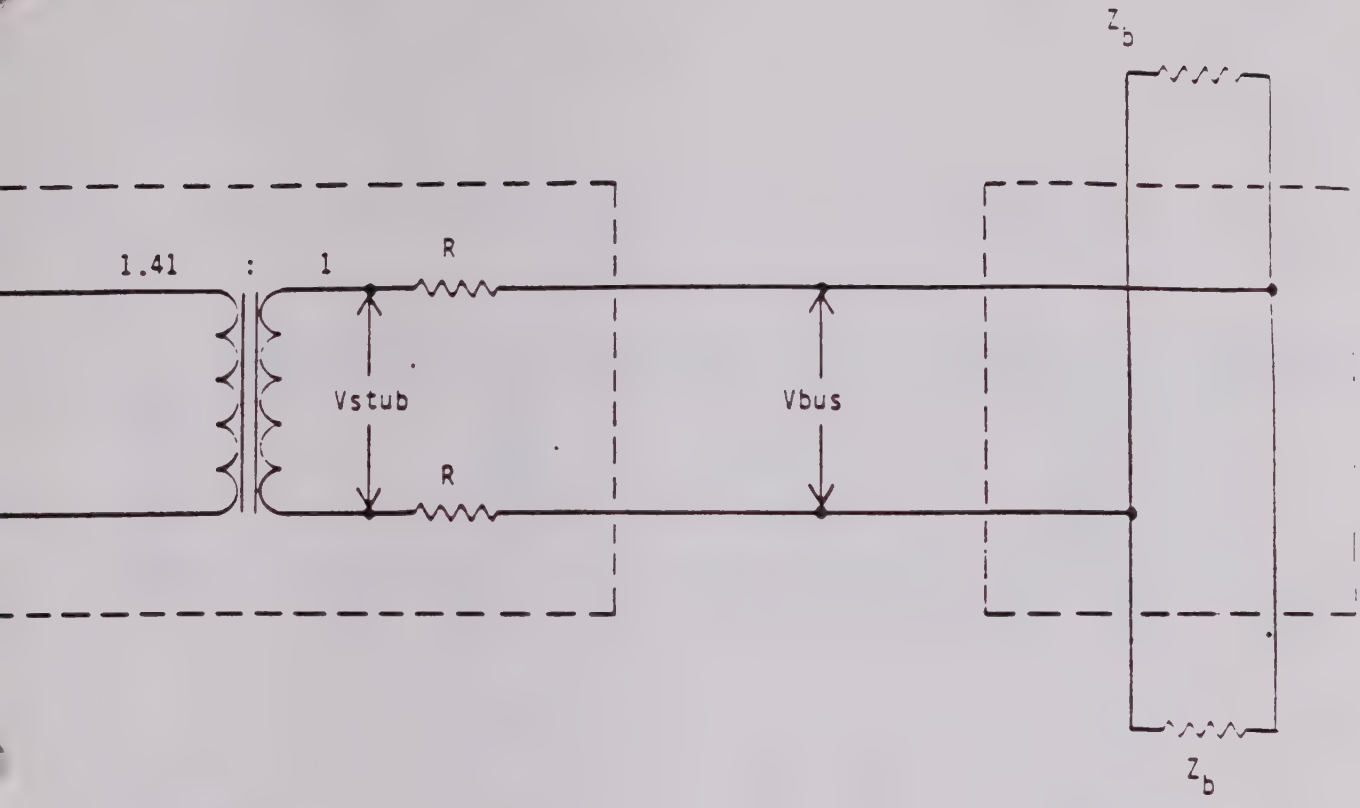
R = 55Ω ±2%
$R_T$ = 38.7Ω ±1%

553A to Instrument

Vbus = 0-6.74 volts
Vstub = 0-6.74 volts

$V_{STUB}$ = 3.5V (Typ)

FIGURE 1B. 1553B DIRECT COUPLING TO THE BUS




Model 553A

1553B Bus Coupler

R = 55Ω ±10%
Zb = 77.5Ω nominal

553A to Instrument

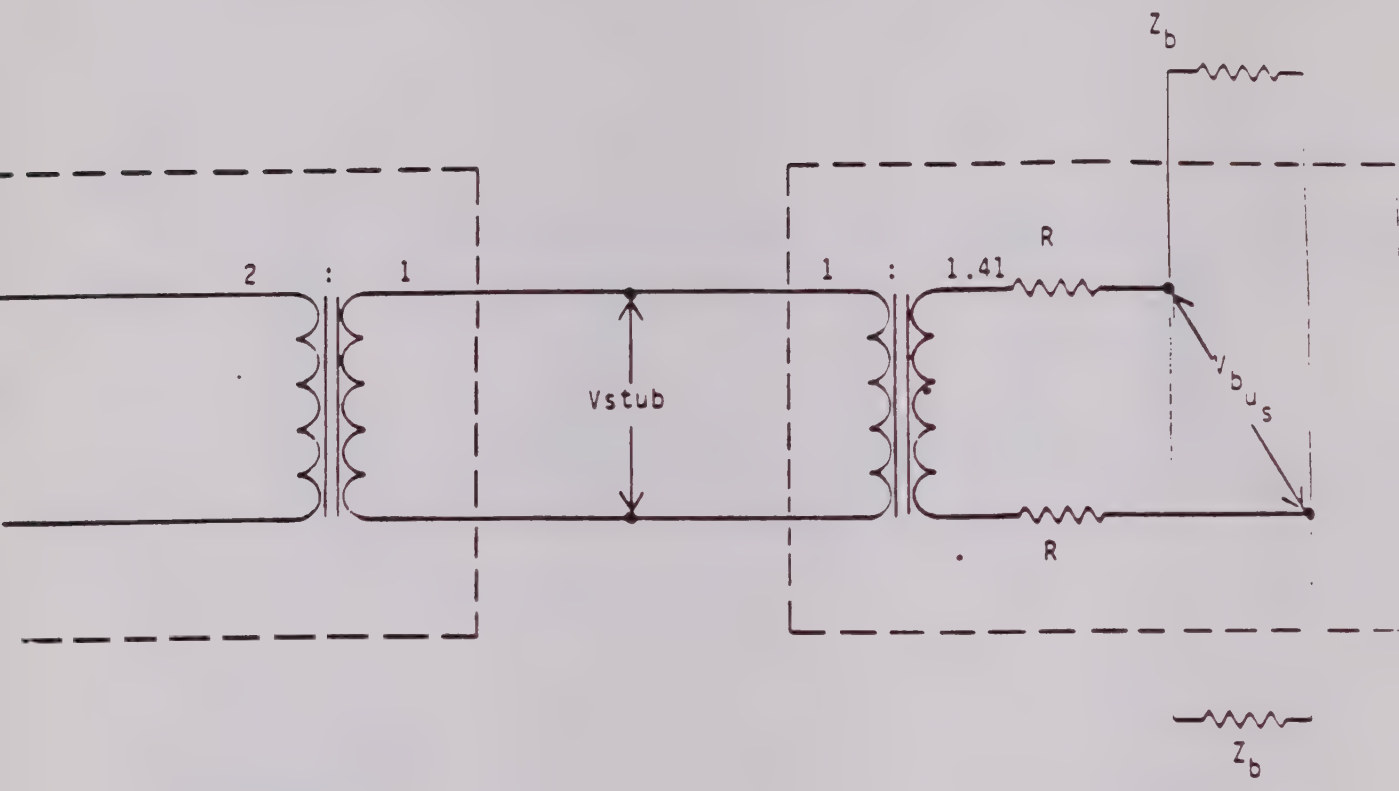
Vstub = 0-27 volts p-p

$$Vbus = Vstub \left[ \frac{Zb/2}{2R+Zb/2} \right]$$

= 0-7.03 volts p-p

$V_{BUS}$ = 3.8V (Typ)

FIGURE 2B. 1553B TRANSFORMER COUPLED TO THE BUS




Model 553A

1553B Bus Coupler

Zb = 77.5Ω nominal
R = 55Ω ±10%

553A to Instrument

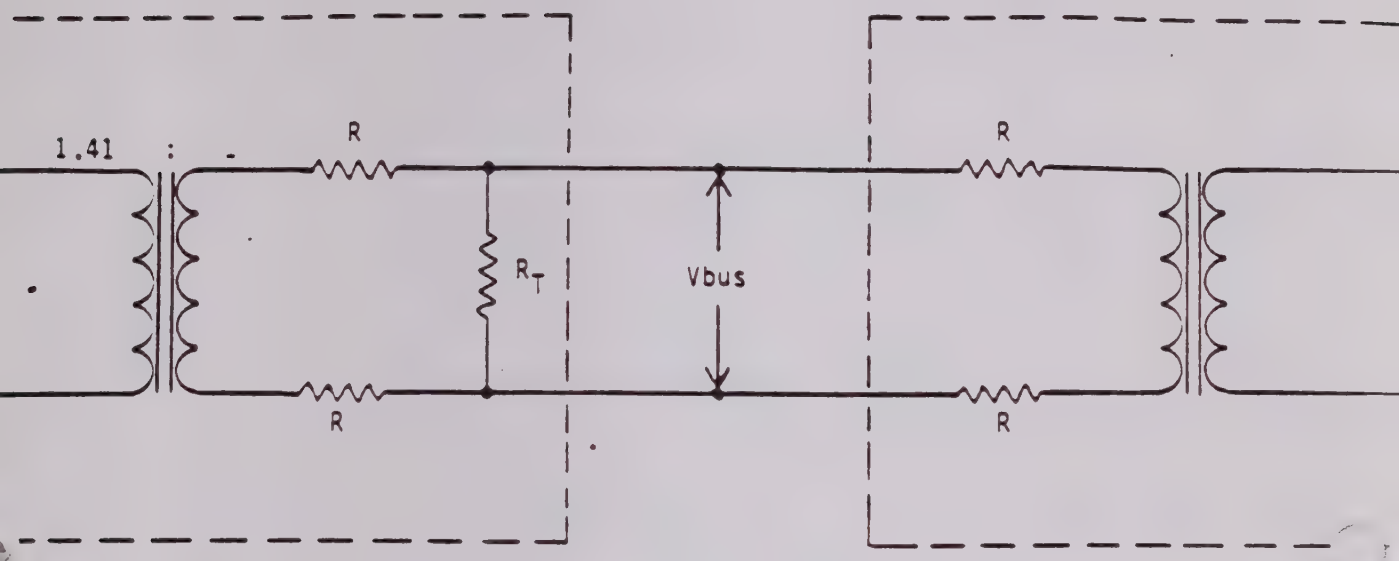
Vstub = 0-20 volts

$$V_{bus} = (V_{stub})(1.41)\left[\frac{Zb/2}{2R+Zb/2}\right]$$

= 0-7.35 volts

$V_{STUB}$ = 11.3V (Typ)
$V_{BUS}$ = 3.5V (Typ)

FIGURE 3B. 1553B DIRECT COUPLED TO AN INSTRUMENT OR LRU




Model 553A

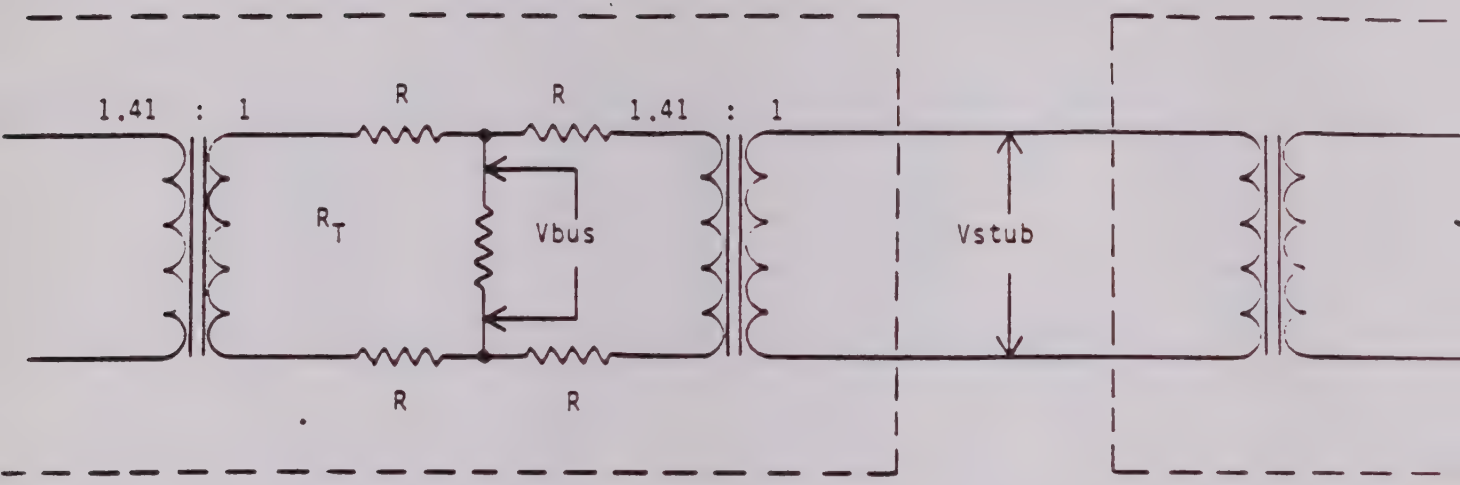
1553B Instrument

R = 55Ω ±1%
$R_T$ = 38.7Ω

553A to Instrument

Vbus = 0-6.74 volts = $V_{STUB}$ $V_{BUS}$ = 3.3V (Typ)

FIGURE 48. 1553 TRANSFORMER COUPLED TO AN INSTRUMENT OR LRU




Model 553A

1553B Instrument

R = 55Ω
$R_T$ = 38.7Ω

553A to Instrument

Vbus = 0-7.03 volts
Vstub = 0-4.99 volts

$V_{STUB}$ = 2.5V (Typ)

# APPENDIX D. MODEL 553A DATA ENTRY ERROR CODES

| ERROR # | DESCRIPTION |
|---|---|
| 00 | EXECUTE NON EXISTENT MEMORY |
| 01 | UNACCEPTABLE INPUT - SHOULD NEVER OCCUR |
| 07 | EEPROM NOT INITIALIZED |
| 08 | INVALID KEY DIRECTORY DISPLAY |
| 09 | INVALID KEY BLOCK DISPLAY |
| 11 | INVALID KEY INPUT STATE |
| 12 | INVALID KEY MENU STATE |
| 13 | INVALID KEY RUN STATE |
| 14 | CONTINUE KEY IN RUN BUT NOT PAUSED |
| 15 | KEYBOARD DECODE |
| 19 | DUAL RAMP FUNCTION (MENU) |
| 19 | DUAL RAMP FUNCTION (EXECUTION) |
| 20 | CAN'T FIND BLOCK |
| 21 | TEST NUMBER UNSPECIFIED |
| 22 | SAVING EMPTY BLOCK |
| 23 | MISSING EEPROM |
| 24 | BLOCK NUMBER ALREADY EXISTS |
| 25 | BLOCK NAME TOO LONG |
| 26 | INVALID NUMBER OF MU PARAMETERS |
| 30 | INPUT STRING LENGTH EXCEEDED |
| 31 | TOO MANY CHARACTERS FOR DISPLAY |

## APPENDIX D. MODEL 553 DATA ENTRY ERROR CODES
(continued)

| ERROR # | DESCRIPTION |
|---|---|
| 32* | USER MEMORY FULL |
| 33* | TN TOO LARGE FOR ACTIVE BLOCK |
| 34* | NO DATA WORD PRIOR TO PR COMMAND |
| 40* | INVALID COMMAND |
| 41* | WORD TOO LONG |
| 42* | INVALID ERROR SPECIFICATION |
| 43* | INVALID CHARACTERS IN TRAP |
| 44* | BIT CELL SPEC MUST BE 1-20 |
| 45* | OUT OF RANGE MENU CONTROL |
| 46* | EXECUTABLE COMMAND IN ACTIVE BLOCK |
| 47* | INVALID MU PARAMETER |
| 48* | INVALID GAP SPEC |
| 50* | INVALID HEX NUMBER |
| 51* | INVALID OCT NUMBER |
| 52* | INVALID DEC NUMBER |
| 60* | EMPTY ACTIVE BLOCK |
| 61* | ENCODER MEMORY OVERFLOW |
| 62* | CAN'T FIND BLOCK NAME |
| 63* | STACK OVERFLOW |
| 70 | EXECUTION ERROR |

Note: * indicates error that will display the command string generating the error.

# APPENDIX E. SELF TEST GLOSSARY AND ERROR DISPLAYS

The following abbreviations are used within the Error Description Table E-1.

| ABBREVIATIONS | MEANING |
|---|---|
| ADR-M<br>ADR-L | Address of test location. Most significant (M) and least significant (L) bytes. |
| DATA-W | Data written to a RAM location. |
| DATA-R | Data read from RAM location. |
| DADRC | Decoder address count (Port D1). |
| DSTAT | Decoder status (Port D0). |
| RSTAT | Received status of word or gap. |
| RDATA-M<br>RDATA-L | Data received. Most (M) and least (L) significant bytes. |
| SDATA-M<br>SDATA-L | Data sent. Most (M) and least (L) significant bytes. |
| SGAPT | Length of gap sent. Time in usecs. |
| RGAPT | Length of gap received. Time corrected for length of sync. Time in eights of usecs. |
| DTCNT | Decoder trap count. |
| ESTAT | Encoder status. |

## TABLE E-1. ERROR DISPLAY DESCRIPTIONS

| TEST NO. | TEST DESCRIPTION | DISPLAYED REGISTER CONTENTS | | | |
|---|---|---|---|---|---|
| | | R0 | R1 | R2 | R3 |
| C00 | RAM | ADR-M | ADR-L | DATA-W | DATA-R |
| C01 | VIDEO RAM<br>SYSTEM CHECKSUM<br>USER CHECKSUM | ADR-M<br>--<br>-- | ADR-L<br>--<br>-- | DATA-W<br>--<br>-- | DATA-R<br>--<br>-- |
| D00 | REGISTER CLEAR | DADRC | DSTAT | X | X |
| D01 | RAM | ADR-M | ADR-L | DATA-W | DATA-R |
| D02 | TRAP RAM | ADR-M | ADR-L | DATA-W | DATA-R |
| D03 | BASIC RCV-ADR CNT | RSTAT<br>X | RDATA-M<br>X | RDATA-L<br>X | DADRC<br>=0 |
| D04 | RECEIVED DATA | RSTAT<br>X | RDATA-M<br>5C | RDATA-L<br>A3 | DADRC<br>X |
| D05 | ERRORS | RSTAT<br>0000XXXX | RDATA-M<br>X | RDATA-L<br>X | DADRC<br>X |
| D06 | DATA SYNC | RSTAT<br>XXXXX0XX | RDATA-M<br>X | RDATA-L<br>X | DADRC<br>X |
| D07 | NO GAP | RSTAT<br>XXXXXX00 | RDATA-M<br>X | RDATA-L<br>X | DADRC<br>X |
| D08 | RECEIVED DATA | SDATA-M | SDATA-L | RDATA-M<br>SDATA-M | RDATA-L<br>SDATA-L |
| D09 | COMMAND SYNC | RSTAT<br>XXXXX1XX | X | X | X |
| D10 | PARITY ERROR-FLAG | RSTAT<br>XXX1XXXX | X | X | DSTAT<br>X |
| D11 | PARITY ERROR-TRAP | RSTAT<br>X | X | X | DSTAT<br>XXXXXXX1 |

TABLE E-1. ERROR DISPLAY DESCRIPTIONS
(continued)

| TEST NO. | TEST DESCRIPTION | DISPLAYED REGISTER CONTENTS | | | |
|---|---|---|---|---|---|
| | | R0 | R1 | R2 | R3 |
| D12 | MANCHESTER ERR-FLAG | RSTAT<br>XX1XXXXX | X | X | DSTAT<br>X |
| D13 | MANCHESTER ERR-TRAP | RSTAT<br>X | X | X | DSTAT<br>XXXXXXX1 |
| D14 | LONG WORD ERR-FLAG FOLLOWED BY WORD | RSTAT<br>1XXXXXXX | X | X | DSTAT<br>X |
| D15 | LONG WORD ERR-FLAG FOLLOWED BY GAP | RSTAT<br>1XXXXXXX | X | X | DSTAT<br>X |
| D16 | LONG WORD ERR-TRAP | RSTAT<br>X | X | X | DSTAT<br>XXXXXXX1 |
| D17 | SHORT WORD ERR-FLAG FOLLOWED BY WORD | RSTAT<br>X1XXXXXX | X | X | DSTAT<br>X |
| D18 | SHORT WORD ERR-FLAG FOLLOWED BY GAP | RSTAT<br>X1XXXXXX | X | X | DSTAT<br>X |
| D19 | SHORT WORD ERR-TRAP | RSTAT<br>X | X | X | DSTAT<br>XXXXXXX1 |
| D20 | SHORT GAP-FLAGS | RSTAT<br>XXXXXX01 | RDATA-M<br>X | RDATA-L<br>X | DSTAT<br>X |
| D21 | LONG GAP-FLAG | RSTAT<br>XXXXXX1X | X | X | DSTAT<br>X |
| D22 | GAP TIME | SGAPT | RGAPT | X | X |
| D23 | TRAP COUNT | SCNT<br>X | DTCNT<br>SCNT+1 | DADRC<br>X | DSTAT<br>X |
| D24 | ADDRESS COUNT | SCNT<br>X | DTCNT<br>X | DADRC<br>SCNT+2 | DSTAT<br>X |

TABLE E-1. ERROR DISPLAY DESCRIPTIONS
(continued)

| TEST NO. | TEST DESCRIPTION | DISPLAYED REGISTER CONTENTS | | | |
|---|---|---|---|---|---|
| | | R0 | R1 | R2 | R3 |
| D25 | ADDRESS COUNT OVERFLOW NOT SET | SCNT<br>X | DTCNT<br>X | DADRC<br>X | DSTAT<br>XXXXXOXX |
| D26 | ADDRESS COUNT OVERFLOW SET | DSTAT<br>XXXXX1XX | X | X | X |
| D27 | TRAP AT END OF DATA | DADRC<br>XXXXXXOX | DSTAT<br>XXXXXX1X | X | X |
| D28 | TRAP AT MIDDLE OF DATA | DADRC<br>80 | X | X | X |
| D29 | TRAP AT BEGINNING OF DATA | DADRC<br>0 | X | X | X |
| D30 | TRAP DATA COMPARE | DTCNT<br>03 | X | X | X |
| D31 | TRAP ON COMMAND SYNC | DTCNT<br>02 | X | X | X |
| D32 | TRAP ON COMMAND SYNC | DTCNT<br>03 | X | X | X |
| E00 | RAM | ADR-M | ADR-L | DATA-W | DATA-R |
| E01 | ENCODER STOP-POC | ESTAT<br>XXXXXXX1 | X | X | X |
| E02 | ENCODER START | ESTAT<br>XXXXXXX0 | X | X | X |
| E03 | ENCODER STOP-AFTER RUN SEQ | ESTAT<br>XXXXXXX1 | X | X | X |
| E04 | BASIC ENCODING | RSTAT<br>0000X000 | RDATA-M<br>AB | RDATA-L<br>X | X |

TABLE E-1. ERROR DISPLAY DESCRIPTIONS
(continued)

| TEST NO. | TEST DESCRIPTION | DISPLAYED REGISTER CONTENTS | | | |
|---|---|---|---|---|---|
| | | R0 | R1 | R2 | R3 |
| E05 | GAP ENCODING | RSTAT<br>XXXXXXX1 | RDATA-M<br>X | RDATA-L<br>X | X |
| E06 | ENCODE WORD FOLLOWS GAP | RSTAT<br>0000X000 | RDATA-M<br>X | RDATA-L<br>CD | X |

# APPENDIX F. CODING FORMS

This appendix contains coding sheets which may be useful for encoding the desired binary data.

F.1 Command Word coding.

F.2 Data Word coding.

F.3 Status Word coding.

## F.1 MODEL 553A COMMAND WORD CODING

### I. MIL-STD-1553A/B FORMAT:

BIT TIMES

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

COMMAND WORD

| | | 5 | 1 | 5 | 5 | 1 |
|---|---|---|---|---|---|---|
| SYNC(1) | | REMOTE TERMINAL ADDRESS | T/R | SUBADDRESS/MODE | DATA WORD COUNT/MODE CODE | P(2) |

(1) Generated by preceding data entry by "CMD SYNC" (K).

(2) Odd parity is automatically generated by Model 553A unless a parity error (P-ERR) is inserted.

### II. CODING FORM:

| BINARY DATA | | | | | HEXADECIMAL ENTRY |
|---|---|---|---|---|---|
| <--RT ADDRESS--> | T/R | <--SUBADDR OR MODE--> | | <--DATA WORD COUNT--> | |
| - - - - | - | - | - - | - - - - | - - - - - |
| 0 0 1 0 | 0 | 0 | 0 0 | 0 0 1 1 1 0 0 1 | K 2 0 3 9 |

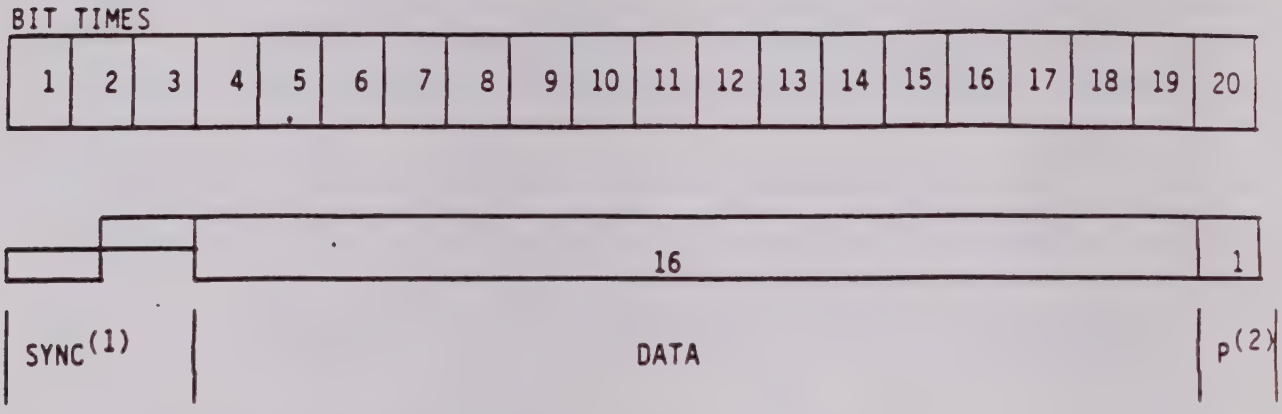
Example: Command to RT4, Subaddress 1 to receive 25 ($31_8$) words.

## MODEL 553A COMMAND WORD CODING SHEET

| BINARY DATA | | | | HEXADECIMAL ENTRY |
|---|---|---|---|---|
| <--RT ADDRESS--> | T/R | <--SUBADDR OR MODE--> | <--DATA WORD COUNT--> | |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |
| _ _ _ _ _ | _ | _ _ _ _ _ | _ _ _ _ _ | K _ _ _ _ |

## F.2 MODEL 553A DATA WORD CODING

### I. MIL-STD-1553A/B FORMAT:




(1) Automatically generated by Model 553A.

(2) Odd parity generated by Model 553A unless a parity error (P-ERR) is inserted.

### II. CODING FORM:

| BINARY DATA | | | | HEXADECIMAL ENTRY |
|---|---|---|---|---|
| ---- | ---- | ---- | ---- | ---- |
| 0001 | 0010 | 0011 | 1111 | 123F |

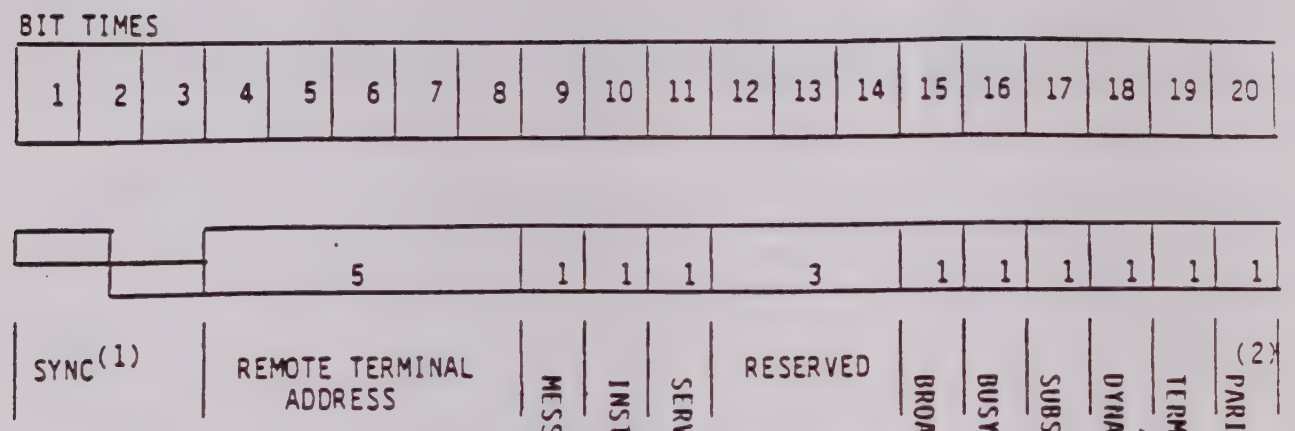
Example: Data word of 123F.

## MODEL 553A DATA WORD CODING SHEET

| BINARY DATA | | | | HEXADECIMAL ENTRY |
|---|---|---|---|---|
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |
| ---- | ---- | ---- | ---- | ---- |

## F.3 MODEL 553A STATUS WORD CODING

### I. MIL-STD-1553A/B FORMAT:




(1) Generated by preceding data entry by "CMD SYNC" (K).

(2) Odd parity generated by Model 553A unless a parity error (P-ERR) is inserted.

II. CODING FORM

| BINARY DATA | | | | | | | | | | | | | | | | HEXADECIMAL ENTRY |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| <--RT ADDRESS--> | | | | | | | | <--RESERVED--> | | | | | | | | |
| _ _ _ _ _ | _ | _ | _ | _ | | | _ | _ | | | _ | _ | _ | _ | | K _ _ _ _ |
| _ _ _ _ _ | _ | _ | _ | _ | | | _ | _ | | | _ | _ | _ | _ | | K _ _ _ _ |

## MODEL 553A STATUS WORD CODING SHEET

| BINARY DATA | | | | | | | | | | | | | | | | HEXADECIMAL ENTRY |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| <--RT ADDRESS--> | | | | | | | <--RESERVED--> | | | | | | | | | |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |
| | | | | | | | | | | | | | | | | K |

# APPENDIX G. 553A THEORY OF OPERATION

## CPU THEORY OF OPERATION

The CPU (Central Processor Unit) circuit board performs all of the non-MIL-STD-1553 input, output and control. The heart of the CPU is a Z80A microprocessor as shown in Figure 1. The MIL-STD-1553 Encoder and Decoder circuit boards are coupled to the CPU through a 50 pin interface connector and ribbon cable. The memory consists of 8K bytes of CMOS RAM and space for 20K bytes of PROM. The Model 553A uses only a part of the memory for operating system, so 7K bytes of RAM and 8K bytes of PROM are available for user programs.

The video contains a small video refresh memory and video controller so that composite video output can drive a display with 16 lines of 32 characters. Through input and output ports the Z80A controls the keyboard, RS-232 and IEEE 488 interfaces. Anytime a character is input on one of these interfaces, the Z80 is interrupted to process the character. An interrupt from the keyboard causes the Z80A to scan the keyboard switch matrix to determine the active key.

## CPU-DETAILED CIRCUIT DESCRIPTION

Components associated with the following circuit blocks are as marked on the attached CPU schematic.

Intercard Connector: The CPU controls the Encoder and Decoder circuit boards through the 50 pin interface connector and a ribbon cable. Though all Z80A signals are buffered and passed to the intercard connector, they are not necessarily used by other circuit boards. See Table 1 for a list of intercard connector pin assignments.

CPU: The CPU itself is a Z80A microprocessor (U30) running at 4 MHz. The address, data and control lines are buffered (U34, U35, U28, U27). The direction of the Data Bus Buffer (U28) is determined by the write line (WR). In order to guarantee that signals into the processor are stable on the rising edge of the clock, they are latched into the register (U33) on the falling edge of the clock. The resistor and capacitor (R4, C13) provide a long time constant for a power on clear (POC). The diode helps force a power on clear if the power is momentarily interrupted. The Schmitt Trigger Buffers (U19) help prevent bouncing of the power on clear.

FIGURE 1. CPU BLOCK DIAGRAM

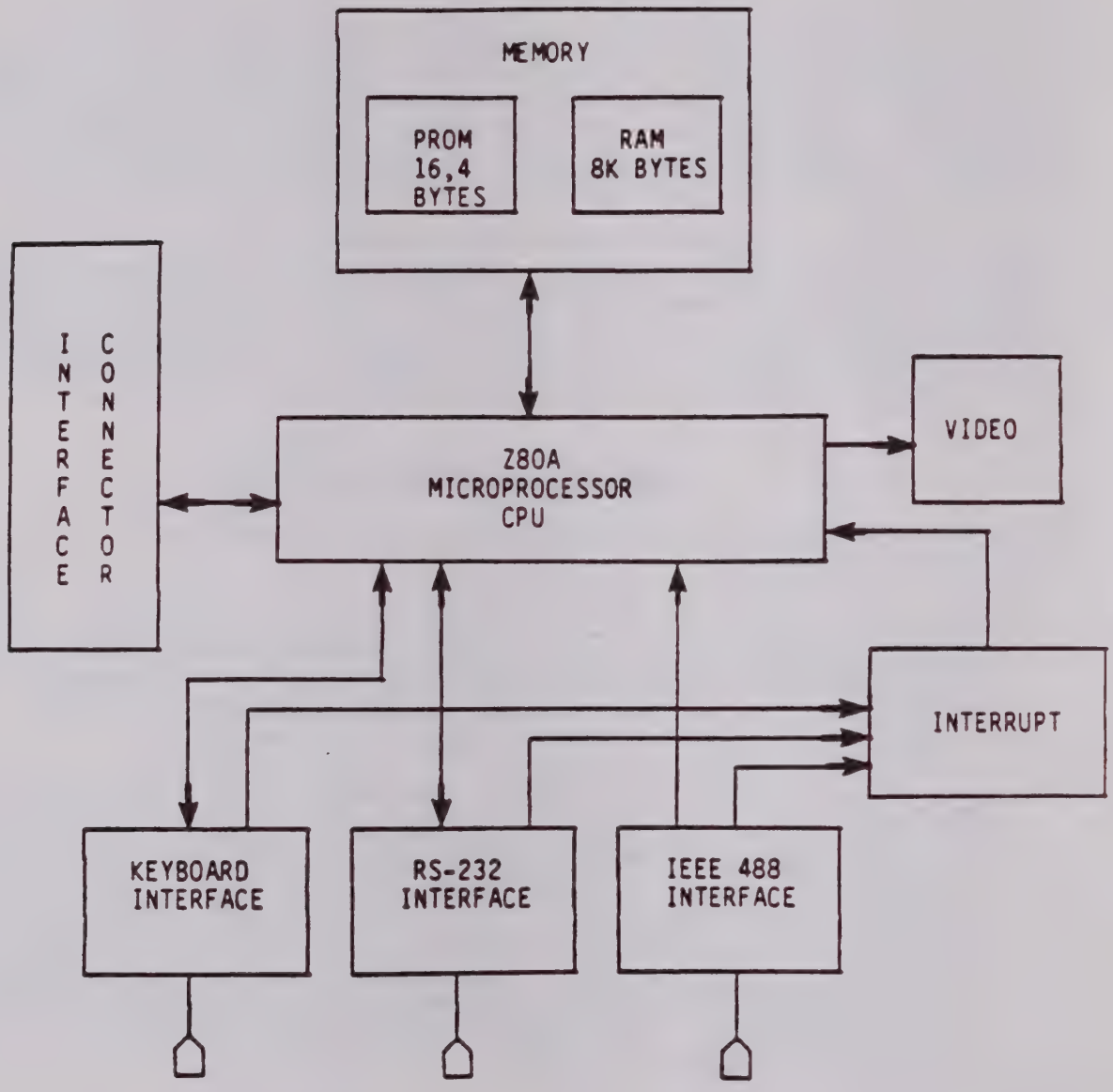


TABLE 1. INTERCARD CONNECTOR PIN ASSIGNMENTS

| PIN | NAME | USED ON | PIN | NAME | USED ON |
|---|---|---|---|---|---|
| 1 | DB0 | CDE | 26 | GND | CDE |
| 2 | DB1 | CDE | 27 | $\overline{\text{IORQ}}$ | C |
| 3 | DB2 | CDE | 28 | $\overline{\text{MREQ}}$ | C |
| 4 | DB3 | CDE | 29 | $\overline{\text{RD}}$ | C |
| 5 | DB4 | CDE | 30 | $\overline{\text{WR}}$ | CDE |
| 6 | DB5 | CDE | 31 | $\overline{\text{BUSRQ}}$ | C |
| 7 | DB6 | CDE | 32 | $\overline{\text{BUSAK}}$ | C |
| 8 | DB7 | CDE | 33 | $\overline{\text{WAITR}}$ | CD |
| 9 | GND | CDE | 34 | $\overline{\text{MI}}$ | C |
| 10 | AB0 | CDE | 35 | $\overline{\text{POC}}$ | CDE |
| 11 | AB1 | CDE | 36 | $\overline{\text{RFSH}}$ | C |
| 12 | AB2 | CDE | 37 | PCLK | C |
| 13 | AB3 | CDE | 38 | $\overline{\text{TRAPD}}$ | DE |
| 14 | AB4 | CDE | 39 | VDL | DE |
| 15 | AB5 | CDE | 40 | GND | CDE |
| 16 | AB6 | CDE | 41 | $\overline{\text{RAM5}}$ | DE |
| 17 | AB7 | CDE | 42 | $\overline{\text{RAM6}}$ | CD |
| 18 | AB8 | CDE | 43 | $\overline{\text{RAM7}}$ | CD |
| 19 | AB9 | CDE | 44 | $\overline{\text{OUTD}}$ | CD |
| 20 | AB10 | C | 45 | $\overline{\text{OUTE}}$ | C E |
| 21 | AB11 | C | 46 | $\overline{\text{IND}}$ | CD |
| 22 | AB12 | C | 47 | $\overline{\text{INE}}$ | C E |
| 23 | AB13 | C | 48 | TRAPP | DE |
| 24 | AB14 | C | 49 | RDATA | DE |
| 25 | AB15 | C | 50 | $\overline{\text{RDATA}}$ | DE |

C = CPU
D = DECODER
E = ENCODER

Memory Control: The Memory Control determines which RAM or PROM chip is to be enabled. See Table 2 for a memory map of the CPU. The Decoder PROM U29 (B5) determines the 4K window of the address when the address is valid (U24). These are the enables for the PROM (ROM1, ROM2) and for RAM and for the other allocated memory. The Memory Buffer (U25) is enabled when MBR=0 (i.e. when a PROM is addressed or when a RAM is enabled.

Memory: The CPU Memory consists of one 27128 EPROM (U9) and two 6264 CMOS RAMs (U15, U16) which are enabled by signals from the Memory Control. The Memory Buffer (U25) is enabled whenever one of the RAMs or PROMs is enabled. The read line (RD) sets the direction of the buffer.

Timing: An 8 MHz crystal oscillator (U17) is divided by two (U18) and buffered (U27) to provide the 4 MHz processor clock (PCLK). A second divider (U18) gives 2 MHz for the RS-232 UART which also uses a clock (URTCK) that is 16 times the baud rate. This baud rate clock is generated by dividing 4 MHz by 13 (U13) and further in steps of two (U7). Baud rate select switch connected through J4 set the Decoder (U1) to select the correct frequency for the desired baud rate.

Port Decoder: The Port Decoder determines the address for a port input (U39) and port output (U37). See Table 3 for a list of the input and output ports.

Keyboard Interface: The keyboard switches are arranged in an undecoded column/row matrix. The columns connect to J8 and are pulled up by resistors (U53). The CPU can read the status of columns via an input from port 90 (U47). The CPU can drive the rows at J8 by doing an output into the register (U50) at port 90. Initially, the CPU sets all rows to zero so that when any key is depressed, one of the column lines (KR0-KR7) is forced to zero, sending an interrupt (U48) to the CPU. In response to the interrupt the CPU executes a procedure of selectively driving the rows and reading the columns until it has determined the active key.

TABLE 2. CPU MEMORY MAP

| ADDRESS (H) | DESCRIPTION |
|---|---|
| 0000-3FFF | PROM1 (16K) |
| 4000-4FFF | PROM4-USER PROM TO BACK PANEL |
| 4800-4FFF | PROM4-USER EEPROM TO BACK PANEL |
| 8000-9FFF | RAM0 |
| A000-BFFF | RAM1 |
| 7000-73FF | RAM4-VIDEO RAM (USES 7000-71FF) |
| 5000-5FFF | RAM5-ENCODER RAM (4K) |
| 7800-7BFF | RAM6-DECODER RAM |
| 7C00-7FFF | RAM7-TRAP RAM |
| 6000-6FFF | UNUSED |
| 7400-77FF | UNUSED |
| C000-FFFF | UNUSED |

NOTE: The PROM and RAM number will change based on the new CPU board layout.

## TABLE 3. INPUT AND OUTPUT PORT DEFINITIONS

### CPU REGISTERS

OUTPUT

1. Port 80: RS-232 data to 8251 UART.
   Port 81: Control for UART (Bits defined by 8251).

2. Port 90: Keyboard row driver.

3. Port A0 to A7: IEEE 488 Controller. Registers and bits defined by TMS-9914A.

4. Port D0 to DF: Assigned to Decoder.

5. Port E0 to EF: Assigned to Encoder.

INPUT

1. Port 80: RS-232 data from 8251 UART.
   Port 81: Status from UART (Bits defined by 8251).

2. Port 90: Keyboard column status.

3. Port A0 to A7: IEEE 488 Controller. Registers and bits defined by TMS-9914A.

4. Port B0: IEEE 488 device address and talk only switches.

   Bit 0: Device Address A1
   Bit 1: Device Address A2
   Bit 2: Device Address A3
   Bit 3: Device Address A4
   Bit 4: Device Address A5
   Bit 5: Talk Only = 1, Normal = 0
   Bit 6,7: 0 Always

5. Port D0 to DF: Assigned to Decoder.

6. Port E0 to EF: Assigned to Encoder.

## TABLE 3. INPUT AND OUTPUT PORT DEFINITIONS
(continued)

### DECODER REGISTERS

INPUT

1. Input Port DO = INO: Decoder Status Buffer.

| Bit | Description |
|---|---|
| 0 | TRAP-Indicates that trap has occurred. |
| 1 | TCOMP-Test complete, memory is full and no more data will be saved. |
| 2 | ADROF-Address Overflow: Set when more than 256 words have passed through decoder since initialized by OUT2. |
| 3-7 | P/U-1. |

2. Input Port D1 = IN1: Address Word Count: 8 bits.

3. Input Port D2 = IN2: Trap Word Count: 8 bits-word count when trap occurred.

OUTPUT

1. Output Port D1 = OUT1: Trap Control Reg.

| Bit | Description |
|---|---|
| 0 | TRAPEN-Trap Enable: Stops the memory after appropriate trap timing. |
| 1 | TSTART-Sets trap word counter to count 255 words after trap. (Positions trap in data at start.) |
| 2 | TMID-Sets trap word counter to count 127 words after trap. (Positions trap in data in center.) |
| 3 | TEND-Stops memory access with trap. (Position trap in data at end.) |
| 4 | TSYNC-Trap on Sync: 0 = Do Care, 1 = Don't Care. |
| 5 | TSPOL-Sync Polarity: 0 = No, 1 = Yes. |
| 6 | TERR-Trap on Error: 0 = No, 1 = Yes. |
| 7 | TRAPDE-Trap on Word: 0 = No, 1 = Yes. |

2. Output Port D2-Out2: Decoder Clear (no data) clears 1) address counter, 2) gap timer, 3) trap register.

TABLE 3. INPUT AND OUTPUT PORT DEFINITIONS
(continued)

## ENCODER REGISTERS

OUTPUT

1. Port-E0: Transmit trigger, starts encoder sequence (no data).
2. Port-E1: Trigger clear (no data).
3. Port-E2: Load trigger control reg.

| Bit | Description |
|---|---|
| 0 | Display Receive Only: Gates off receiver while transmitting. |
| 1 | Fast Repeat: Permits fast internal or external repeat. |
| 2 | External Trigger Select: Trigger to be external. |
| 3 | RT Mode: Trigger will occur after trap. |

4. Port-E3: Relay Control Port: Matrix defines bits.
5. Port-E4: Transmit amplitude adjust.
6. Port-E5: Zero crossing adjust.

INPUT

1. Port-E0: Encoder Status.

| Bit | Description |
|---|---|
| 0 | Stop-Encoder Stopped. |
| 1-7 | 0 |

Interrupt: An interrupt can come from the RS-232 (URTINT), IEEE 488 (IEINT) or the keyboard interface (KEYINT) circuit. When an interrupt is received by the priority interrupt Encoder (U41), an interrupt is passed to the Z80A (INT) and a restart address is generated and passed to the Z80A CPU through the buffer (U40) in response to interrupt acknowledge (IORQ and M1 through U29, U23).

RS-232: The RS-232 protocol is handled essentially by the universal asynchronous receiver transmitter (UART, U11). The RS-232 positive and negative signals are converted to and from TTL level by the buffers (U3, U4). The UART is initialized by writing the control information to port 88 (i.e. AB3 = 1). Similarly, UART status is read from port 88, while data is passed via port 80. Both port 80 and 88 use URTRD and URTWR; it is the state of AB3 that differentiates between ports 80 and 88. When a character is received by the UART and is available to be read by the CPU, an interrupt is sent to the CPU (URTINT). The same signal (RXRDY) which generated the interrupt is used as a handshake signal for not clear to send (RCTS) (i.e. don't send another character until the CPU has read this one). The UART uses two clocks: one for internal processes (2M = 2 MHz) and one which is set by timing to be 16 times the RS-232 baud rate (URTCLK).

Video: The video display consists of a 512 character memory, a video controller and an amplifier. The output of this circuit is composite video for the CRT monitor. Each of the 512 active memory locations represent one specific character location on the CRT screen which is formatted as 16 lines of 32 characters. The CPU can read and write to the video memory (U43, U44) through the buffer (U42). When the CPU address indicates an access to video memory (RAM4), the buffers (U45, U49) enables the less significant bits of CPU address onto the memory while disabling the refresh address from the video controller. The gates (U38, U36) provide the write signal from the CPU to video memory. When the CPU is not accessing the video memory, the video controller is reading all 512 memory locations sixty times per second. This data is processed and output (VID) as composite video to be amplified by the emitter follower (2N2484) which is capable of driving the 75 ohm input impedance of the CRT monitor. A crystal oscillator (U52) provides the 3.579 MHz (VCLK) for the video controller.

IEEE 488: The General Purpose Interface Bus (GPIB, IEEE 488) controller (U12) is coupled to the bus (J3) through the buffers (U5, U6). The CPU communicates with the controller's 8 read and write registers at ports A0 through A7. The Port Decoder provides the most significant nibble (AX) of the port address (IEWR, IERD) through gates (U36, U38) to the controller, which decodes the least signifi-cant nibble of the port address from the three address lines (AB0, AB1, AB2). The CPU reads the device address and talk only switches from J4 through the buffer (U14) at port B0. The CPU then transfers these to the appropriate register in the controller. Once initialized, the controller provides the processing necessary to maintain correct protocol on the IEEE 488 Bus. When a character is received by the controller, an interrupt (I488) is sent back to the CPU which must then read the character from the controller before another character can be received. It should be noted that if the controller is not installed in the circuit board, the keyboard will be disabled with an apparent local lock out when the CPU reads the open circuit.

## DECODER THEORY OF OPERATION

The purpose of the Decoder is to process and store data received from the MIL-STD-1553 Data Bus so that it may be read by the CPU.

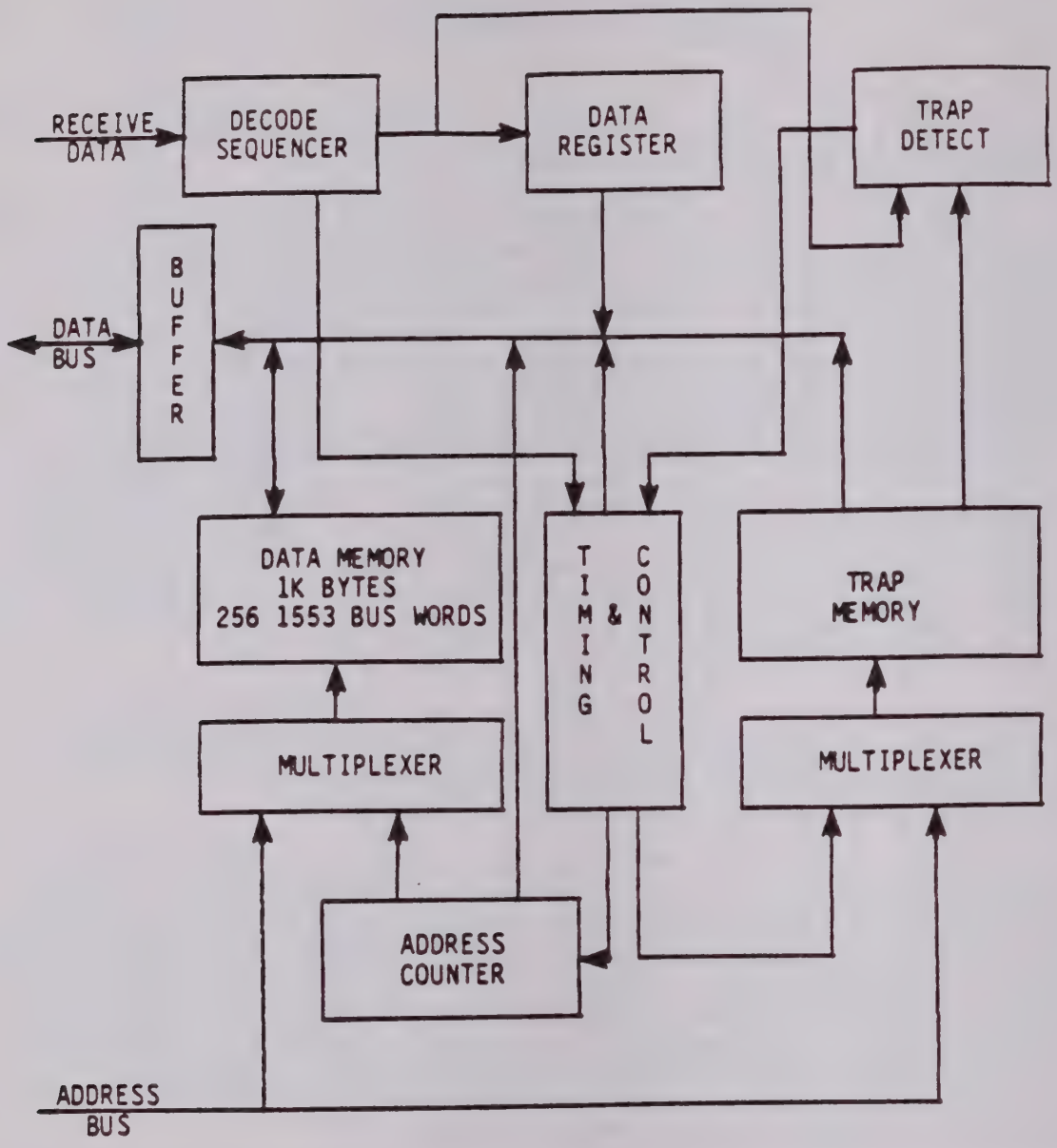
Data are converted from the biphase encoding of the 1553 Bus to two TTL level signals by the 8559 transceiver hybrid on the Encoder board. These two signals, shown as Received Data in the block diagram in Figure 2, are processed by a high speed Decode Sequencer which a) detects a 1553 sync, b) determines bit polarity, c) detects Manchester errors, d) provides a synchronization signal for the Timing circuit and e) detects dead line (no signal on bus). The Decode Sequencer processes data in a 1 microsecond window. Data is shifted into the Data Register by the Timing and Control circuit as synchronized by the signal from the Decode Sequencer. In addition, the Timing and Control circuit counts the number of bits in a word and detects and/or stores various status information (sync polarity, errors, etc.) about the word. When the Decode Sequencer detects a new word or a dead line, the previous word is written to Data Memory by the Timing and Control function. Two bytes of data from the Data Register and one byte of status from the Timing and Control Register are written for each 1553 word. A dead line on the 1553 Bus is timed by the Timing function as long as the gap is shorter than 32 microseconds (called a short gap).

A gap is treated as a Decoder word so that the gap time is written into the Dat Memory. Two bits of the status byte are used to indicate a gap and whether i is a long gap (too long for valid time count). The eight bit gap time is stored as one byte with resolution to an eighth of a microsecond.

A Trap circuit has on and off control of data storage. A trap word in the Trap Memory defines the 16 bits of a word as zero, one or don't care. Each bit of the received words is compared by the Trap Detect circuit with the corresponding bit in the Trap Memory. When all the bits match, a signal is sent to the Timing and Control circuit which then either a) stops receiving data, b) permits 127 more words of data or c) permits 255 more words of data to be received, depending upon the desired position of the data in relation to the trap (i.e. before the trap, centered on the trap, or after the trap). The sync polarity of the trap word is also compared by the Trap Detect. A word error (parity, Manchester, or word length) can be set as the trap.

The CPU can access the Data and Trap Memories through the Address and Data Buses. Multiplexers are used to select between the CPU Address Bus and internal addressing. The 1024 byte Data Memory can store 256 words (bus words and gaps). Three of the four bytes per word are used for bus words and only two bytes for gaps. The Address Counter points to the next available word location in Data Memory. A buffer provides controlled isolation between internal Decoder data and CPU data.

FIGURE 2. DECODER BLOCK DIAGRAM



## DECODER-DETAILED CIRCUIT DESCRIPTION

Components associated with the following circuit blocks are as marked on the attached Decoder schematic.

Address Counter: The Address Counter counts Decoder words and provides the 8 most significant bits of address for the Data Memory. It is clocked at the end of each Memory Access by IQ1. Flip flop U36 is set when at least 256 words have been received.

Address Count Buffer: The Address Count Buffer provides a port through which the CPU can read the contents of the Address Counter.

Trap Address Count Register: When a trap word is detected, the Address Count of the trap word in memory is clocked into the Trap Address Count Register by TRAP. This value may then be read by the CPU.

Address Multiplexer: The Address Multiplexer selects address for the Data Memory from either the Address Counter or the CPU Address Bus. The CPU Address is always selected except when an internal Memory Access switches the Address Multiplexer with IQ1.

Data Memory: Decoded data is stored in the 1024 byte Data Memory at the rate of 4 bytes per Decoder word. Various gates provide the Memory Control from the CPU or Memory Access Timing circuit.

Data Memory Buffer: Read and write access to the Data Memory by the CPU is through the bidirectional tri-state Data Memory Buffer.

Data Register: 16 bits of data (DDATA from the Decode Sequencer) are shifted into the Shift Register (U50, U56) by SCLK (from the Bit Counter). This data is transferred to the register (U51, U57) at the start of a Memory Access by IMRQ, freeing the Shift Register for the next word. Under control of the Memory Access Timing, the data is moved to the Data Memory.

Gap Timer: When a 1553 dead line (DEAD) is detected, the 8 Bit Counter (U43) times the gap. It is clocked at 8 MHz and therefore can measure gaps up to 32 microseconds long. For gaps longer than 32 microseconds, the count overflows into the flip flop (U36) to indicate a long gap. Memory Access Timing latches the count into the register (U44) and transfers it to the Data Memory. The counter is cleared at the end of the Memory Access by MTCLR.

Word Status Register: Various characteristics of the current Decoder word are latched by IMRQ at the beginning of a Memory Access into the Word Status Register. The Memory Timing circuit moves the status from this register into Data Memory.

Trap Memory Address Multiplexer: The Trap Memory may be accessed by either the CPU or by Decoder functions. When the trap is enabled (TRAPEN) in the Trap Control Register, the Trap Memory Address Multiplexer selects the Bit Count as the source of the address.

Trap Memory: The specification for the 16 bits of the trap word are stored in the Trap Memory. Only the two least significant bits of each memory location are used. Each memory location corresponds to one bit of the trap word. The two bits in the memory location set the corresponding bit in the trap word as a don't care (00), zero state (10) or a one state (11). When the trap is enabled, the address to the Trap Memory comes from the Bit Count. Various gates provide control of the Trap Memory.

Trap Memory Buffer: The CPU may read and write to the Trap Memory through the tri-state Trap Memory Buffer.

Trap Control Register: The CPU must set various trap characteristics in the Trap Control Register. TRAPEN enables the trap. The position of the trap in relation to the data is set by TSTART, TMID and TEND. A don't care sync polarity is set by TSYNC, otherwise, the polarity of the trap word sync is set by TSPOL (0 = data sync, 1 = command sync). TERR will cause a trap on an error and TRAPDE enables the Trap Detect to trap on the data as set in the Trap Memory.

Decoder Status Buffer: The CPU reads the status of the Decoder through the Decoder Status Buffer. ADROF is the address overflow from the Address Counter, which is used by the CPU to determine the starting Address Count for the display. TCOMP flags the completion of a test (i.e. Data Memory is full according to the trap specifications). TRAP indicates that the trap word has been detected.

Port Decoder: The CPU reads and writes to various registers at Port Address 0DXH, where the X is determined from the CPU Address (AB0, AB1) by the Port Decoder.

Decode Sequencer: The Decode Sequencer has the following general functions: a) detects a 1553 sync, b) determines bit polarity, c) detects Manchester errors, d) provides a synchronization signal for the Timing and Control circuits. A flip flop (U1) converts the received data signals (RDATA, RDATA) from the transceiver on the Encoder to a polarity (POL). Since RDATA and RDATA can both be simultaneously inactive, the polarity is defined by the last active

signal and is sampled and shifted at an 8 MHz rate into the Shift Register (U7). The eight samples in the Shift Register provide a moving 1 microsecond window which is applied as the address to the synchronization PROM (U13). This PROM provides the following information about the signal in the window: a) CDATA-most probable polarity of Manchester encoding (some sample combinations are indeterminate, so the polarity is arbitrary for these, b) MERR-no transition or three or more transitions between samples constitute a Manchester error, c) DSYNC-all samples high or low could be part of a sync, d) XSYNC-possible exact middle of a sync when the first four samples are of one polarity followed by the remaining sampels in the opposite polarity, e) MSYNC-possible middle of sync when only one or no transitions occurs in the window. The CDATA and MERR signals are stabilized by latching them into register U15. The remaining three signals, along with dead line (DL), are used as inputs to the sequencer (U8, U14) which runs at 8 MHz. The input signals and the next state are latched into the register U8. Based on the latched input signals and the current state, the PROM (U14) outputs next state and control signals. The sequencer has the function of continuously looking for a sync. It executes an algorithm of looking for several DSYNC signals, then an XSYNC, then more DSYNC before declaring that a valid sync (VALS) has been detected. The control signals, along with the CDATA and MERR, are then latched into register U15. The latched and delayed valid sync signals (VS, VSD, VSD2) are the key to establishing the timing for the rest of the word.

Bit Cell Timing: The delayed valid sync (VSD) from the Decode Sequencer synchronizes the Bit Cell Timing to output a pulse (BCKL), which is used to control the sampling of data (i.e. the moving window in the Decode Sequencer will be perfectly positioned over a data bit cell when BCLK occurs). Clocked at 8 MHz, the 8 Bit Counter (U10) puts out a pulse once per microsecond which is then gates with 8 MHz to give the 62 nsec. wide BCLK every microsecond.

Bit Count: The continuous synchronized bit clock (BCLK) from the Bit Cell Timing is counted and gated by Bit Count. The counter is cleared by the delayed valid sync (VSD2) and provides a Binary Count (CA0-CA4) of the current bit within the word. This is used as the Bit Address in the Trap circuit (Trap Memory). Additional Bit Counting takes place as carry from U39 is shifted through the register U33 which gives the timing used for measuring word length and for gating (U29) the clocks for DCLK and SCLK. As a result, DCLK will have 17 and SCLK will have 16 pulses per word.

Dead Line Detect: When neither RDATA nor RDATA signals from the receiver on the Encoder are active, the 1553 line is considered to be dead (DL) by gate U1. The dead line signal (DL) is sampled by Shift Register U2 and when at least four samples in a row are dead (1/2 microsecond), the line is declared very dead (VDL) by gate U3.

Miscellaneous Latches: It is necessary for the Decoder to save the state of various transitory signals which it does in the block of circuits called Miscellaneous Latches. The polarity of a received sync is clocked by the SYNPOL signal from the Decode Sequencer into latch U16. A short time later when the rest of the sync is validated (VS), the Memory Access Timing clocks (IQ1) this polarity into U16, freeing U16 for the next sync.

If a Manchester error is detected by the Decode Sequencer, the JK flip flop U11 will be set. Note that the clock (DCLK) occurs when the 8 sample window in the Decode Sequencer is properly positioned over a data bit cell (i.e. where no Manchester error signals (MERRD) should normally be output).

The parity JK flip flop (U9) is cleared (VSD) at the beginning of every word. Each data bit with a polarity of one will cause this circuit to change state. At the end of a word, the JK should be set (PERR = 1) indicating correct odd parity. A parity error will leave PERR = 0.

The first very dead line (VDL) after the start of a word will set the JK flip flop (U9) to DEAD. This stays set until another valid sync (VS) is detected at which time the DEAD signal is transferred to latch D19B where it becomes GAP, and then DEAD is cleared by valid sync delayed (VSD). If DEAD is active and very dead line (VDL) is not, then GAPIN signals the Word Status Register through gate U18 that the Memory Access is for a gap.

If the Decode Sequencer fails to detect a sync after getting at least part way through, the NOISED signal will be output and latched into U11 as NOISEL, which is then used as one bit of the word status. Though this bit is not displayed to the user, except in a DUMP format, it is used to indicate a noisy line during a gap.

Long Word Detect: The length of words are verified so that errors will be indicated in the Word Status and to set the trap. The length of a word cannot be tested until either the start of another word or the start of a gap indicating the end of the previous word. The timing for a word following is different than for a gap following. In either case, the word length condition is latched by the Memory Access signals (IMRQ in the Word Status Register and IQ1 in the Trap Detect).

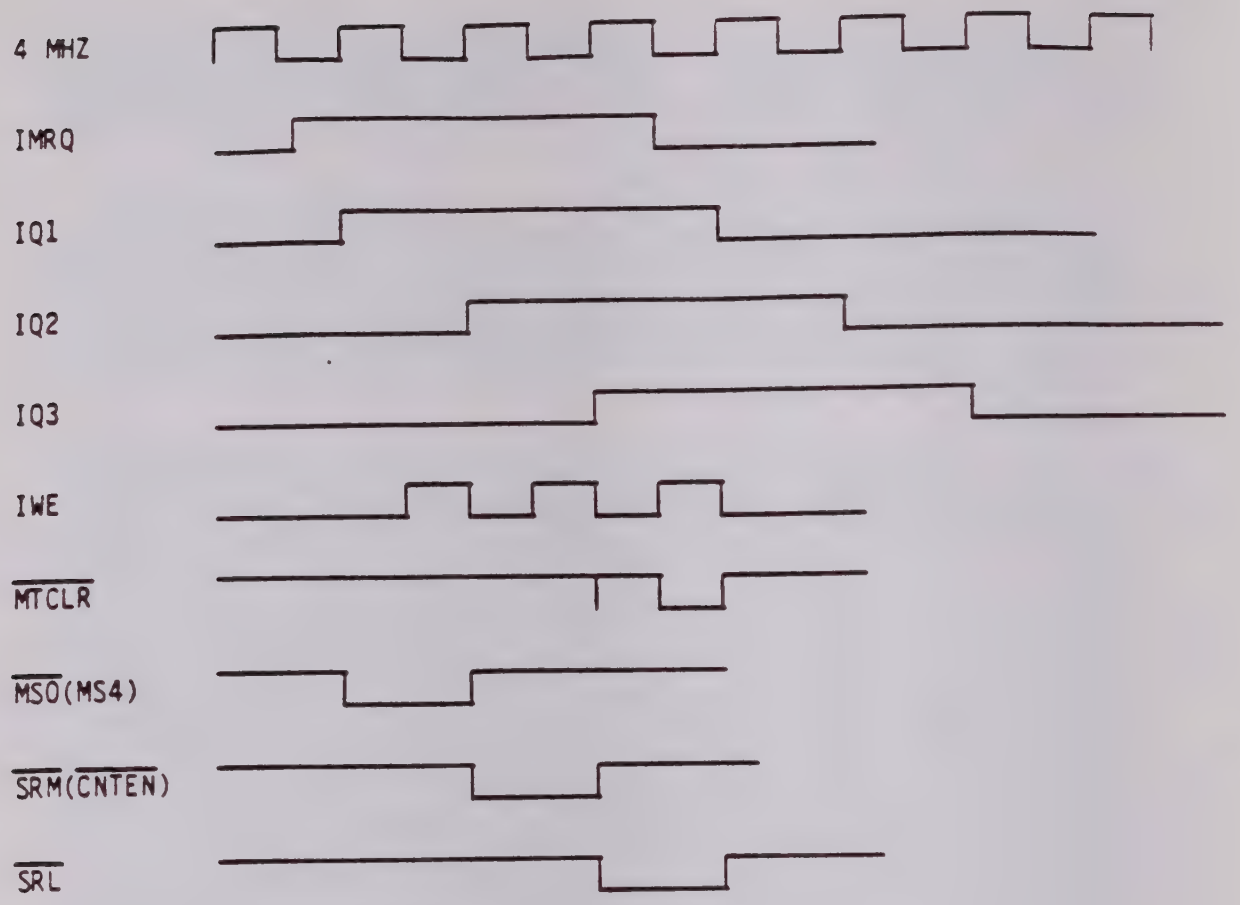
The output of Long Word Detect is signal LGD. If the word is followed by a gap (indicated by VDL) and signal B18 from Bit Count is active, then the word was too long. The JK flip flop (U34) is used to extend Timing Signal B20 by about one half microsecond to create signal LG20. If a valid sync from a new word has not been received by the time LG20 goes active, the word is too long.

Short Word Detect: The general statements about Word Length Timing in the Long Word Detect description (above) also applies to Short Word Detect. The output of this circuit is called SHORT. If a valid sync for a new word is detected (indicated by VDL) and Timing Signal B19 is not active, then the word is too short. Similarly, if a Memory Access occurs (say from a gap) prior to signal B17 going active, the word is too short.

Memory Access Timing: After the start of each word or gap, a Memory Access will occur to record the previous word or gap. The Memory Request (IMRQ) is initiated when latch U23 is set by the rising edge of DEAD or by the valid sync pulse (VS). If the CPU is accessing the Decoder Memory, the internal Decoder Memory sequence will not start until the CPU has completed the access. This conflict is resolved by gate U18 which when ready, starts the Memory Timing in the register U12. The signal is shifted through U12 to provide timing at 250 nsec. intervals (see Figure 3). Three write pulses (IWE) for the Decoder RAM are derived by gating (U18) IQ1 with the 4 MHz clock. Normally, the Timing circuit is reset and ready for another access when the MTCLR signal is wrapped back and clears U23. If the Trap Word Counter indicates (via ITR) that the Decoder Memory is full, the MTCLR will be gated off (U17B), preventing further internal Memory Access.

When the Decoder is internally accessing its memory and the CPU tries to access it, the gates (U18B, U22C, U27A) generate a wait to the CPU. Three bytes of information are written during each Memory Access sequence. The Decoder (U6) enables the registers which contain the data to be written. When the access is to write word information, the word status (MS0), the most significant byte of data (SRM) and the least significant byte of data (SRL) are written in that order. Though only three words are written, a block of four memory locations are used. There is an unused byte between the two data bytes. When a gap is recorded, only the first two bytes are used for status (MS4) and gap time count (CNTEN). The Word Status Register is enabled (STEN) by either word or gap access (U17C).

FIGURE 3. MEMORY ACCESS TIMING



Trap Word Counter: The Decoder Data Memory has a capacity of 1024 bytes and used 4 bytes per Decoder word giving a capacity of 256 words. The Trap Word Counter counts words in relation to the trap word and then disables (ITR) the Memory Access Timing after the correct number of words. The trap position (TEND, TMID, TSTART) is set in the Trap Control Register. If TEND is set, the trap word will be the last word saved in memory. TEND and TRAP (U19, U31) cause the latch (U34) to be set on the Memory Access (IQ3). The output of U34 causes the memory to be disabled (ITR) through gate (U26). When the trap word is to be placed at the start (TSTART) of the received data, the counter (U45, U38) is cleared through gate (U52) by TRAP and TSTART. The counter can count 255 more words before the carry (TCC) disables the Memory Access Timing (ITR). Similarly, the counter (U45, U38) is loaded with 128 when the trap occurs with TMID selected (U52). This permits 127 more words to be received before the counter's carry disables the Memory Access Timing. In all of these cases, the memory will continuously store received data until disabled by the Trap Word Counter.

Trap Detect: The Trap Detect circuit can be set to trap on a particular word, an error, or a combination. There are two outputs from the Trap Detect. One is a pulse (TRAPP) for each occurrence of a trap and the other (TRAP) is continuous after the first occurrence of a trap. Both are linked to the Memory Access Timing, so once Trap Word Counter disables the Memory Access Timing, these signals (TRAPP and TRAP) will be disabled until the Decoder is cleared (OUT2) with an OUT 0D2H from the CPU. The JK flip flop (U21) latches the trap condition. TRAPP is 0.5 usec. long since U21A is cleared just after being set by the Memory Access Timing.

All error conditions are gated together (U38) and if a trap on error (TERR) is selected, this signal passes through gates (U26, U19, U20) to the output flip flops. When trap on word (TRAPDE) is selected, the trap is a combination of the sync and data within the word, any of which can be a don't care. The sync is specified in the Trap Control Register (TSYNC = 1 = X or don't care, TSYNC = 0 = do care, TSPOL = 0 = data sync, TSPOL = 1 = command sync). Comparison of the specified sync TSPOL with the received word sync (WDSYNC) occurs in U32; it is then ORed with the sync don't care signal (TSPOL) in U31. Data is compared serially, bit by bit. The Trap Memory holds the spe-cifications for each bit (TDX = 0 = don't care, TDX = 1 = do care, TDP = 0 = 0 data, TDP = 1 = 1 data). The Bit Count circuit supplies the Trap Memory with the address of the current bit cell. Comparison occurs in U32 and U17.

The JK flip flop (U24) is cleared at the beginning of each word. If it remains cleared throughout the word, then all bits have matched the specified bit pattern. The flip flop will be set by an incorrect match (JTD) when clocked by the data clock (DCLK). The output of the flip flop (U24) is combined with the trap on data control (U26) and the sync (U20) to give the trap on word signal (TPW) to be combined (U27) with the trap on error signal (TPE). The data trap is disabled by a signal from the Encoder (TRAPD) by keeping the flip flop set (TRAPD). This disables the Trap circuit while the Encoder is transmitting in the RT Simulator Mode to prevent false traps from transmitted data.

Refer to Figure 4 for a sample trap circuit timing diagram. Figure 5 illustrates the relationship between access and trap timing.

FIGURE 4. SAMPLE TRAP CIRCUIT TIMING

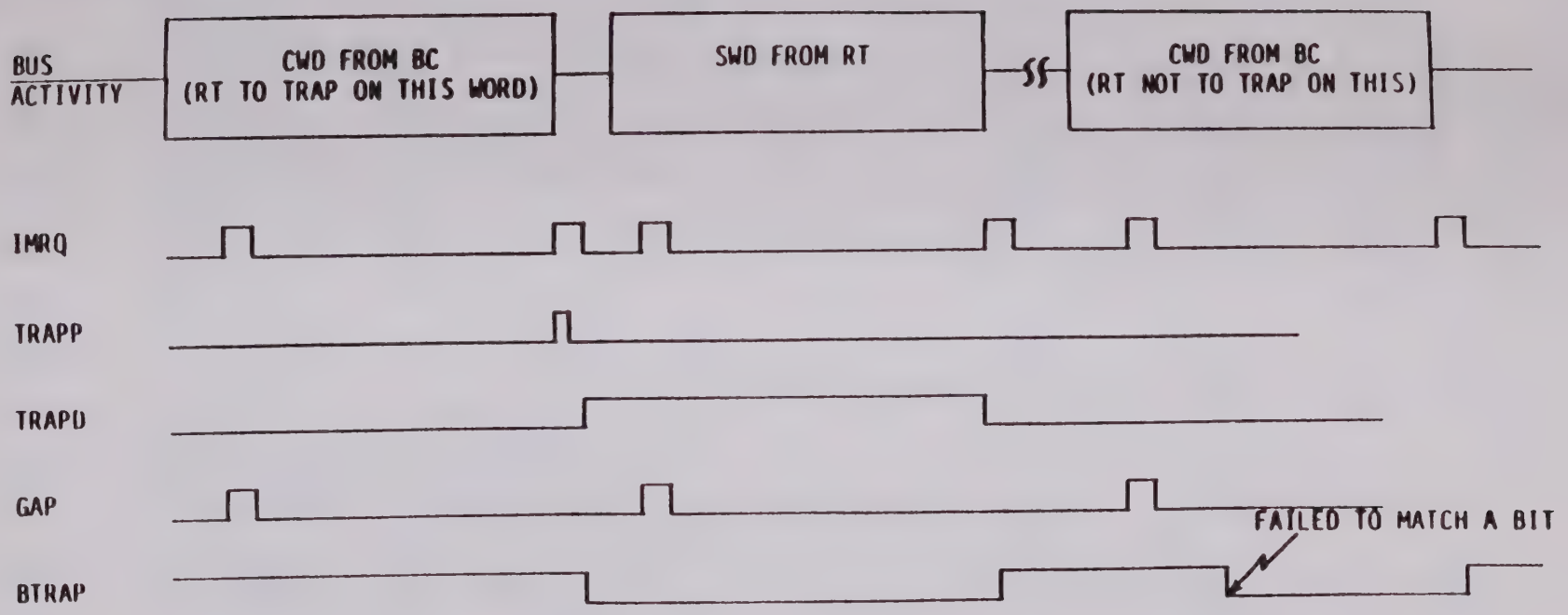
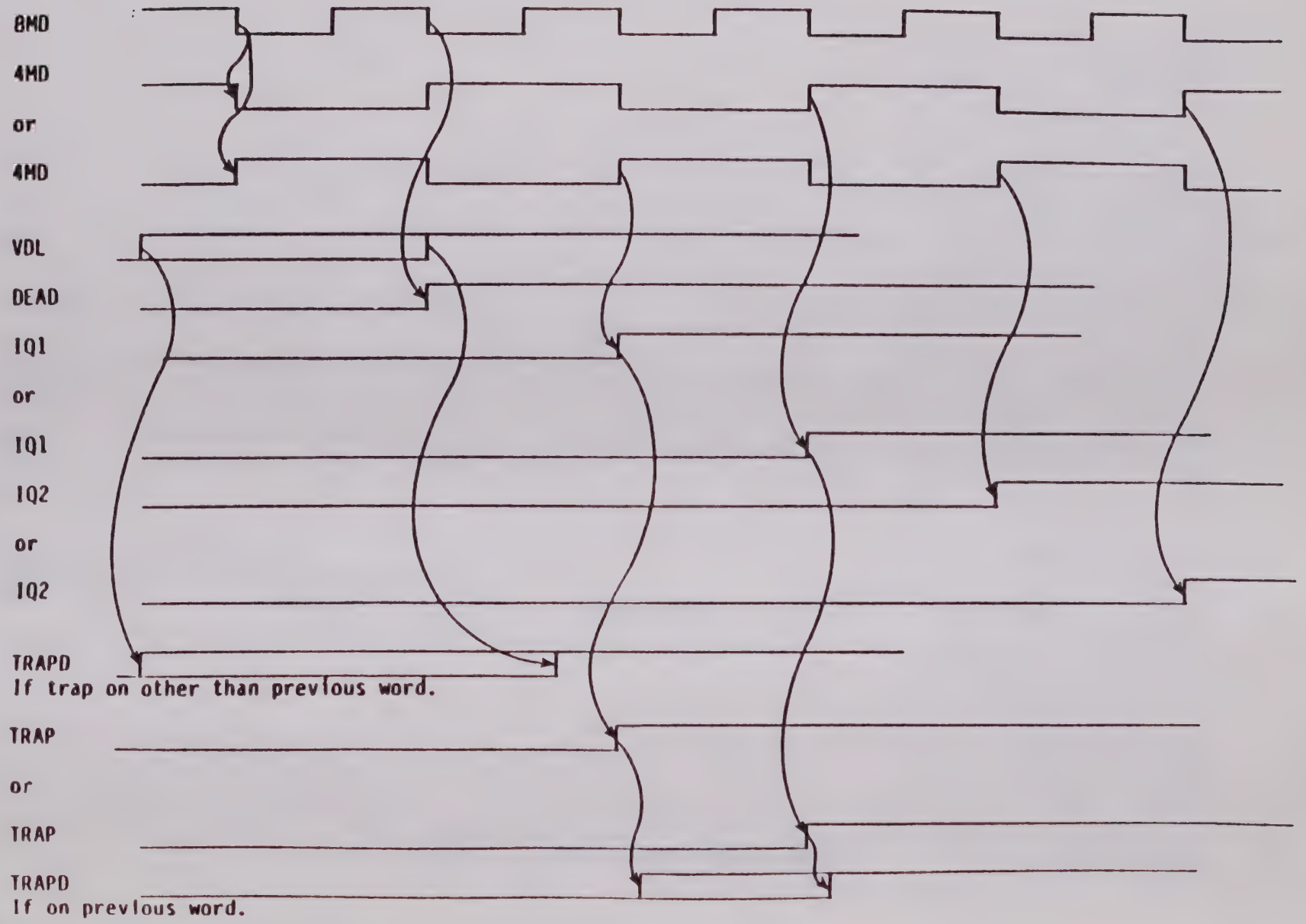


FIGURE 5. MEMORY ACCESS VS. TRAP TIMING



## ENCODER THEORY OF OPERATION

The Encoder circuit board provides the two basic functions of:

a) interfacing with the MIL-STD-1553 Data Buses, and
b) transmitting data in the MIL-STD-1553 Data Bus.

A simplified block diagram of the Encoder is shown in Figure 6.

The interface to the MIL-STD-1553 Data Bus consists of the transceiver and Termination circuit. The transceiver is a hybrid circuit with transmitter and receiver sections which convert TTL signals to 1553 signals and vice versa. The received signals are passed to the Decoder. The 1553 termination and bus selection is accomplished by the CPU setting the state of various relays.

The Encoder processes data to be transmitted on a bit by bit basis. Each byte in memory represents one microsecond (bit) of time on the 1553 Data Bus. The CPU is responsible for formatting and loading the proper data into the Encoder Memory. Each byte contains information about:

a) the state of the first and last half of the bit cell,

b) control of the zero crossing at the center and end of the bit cell,

c) whether the transmitter should be enabled (disabled for gaps), and

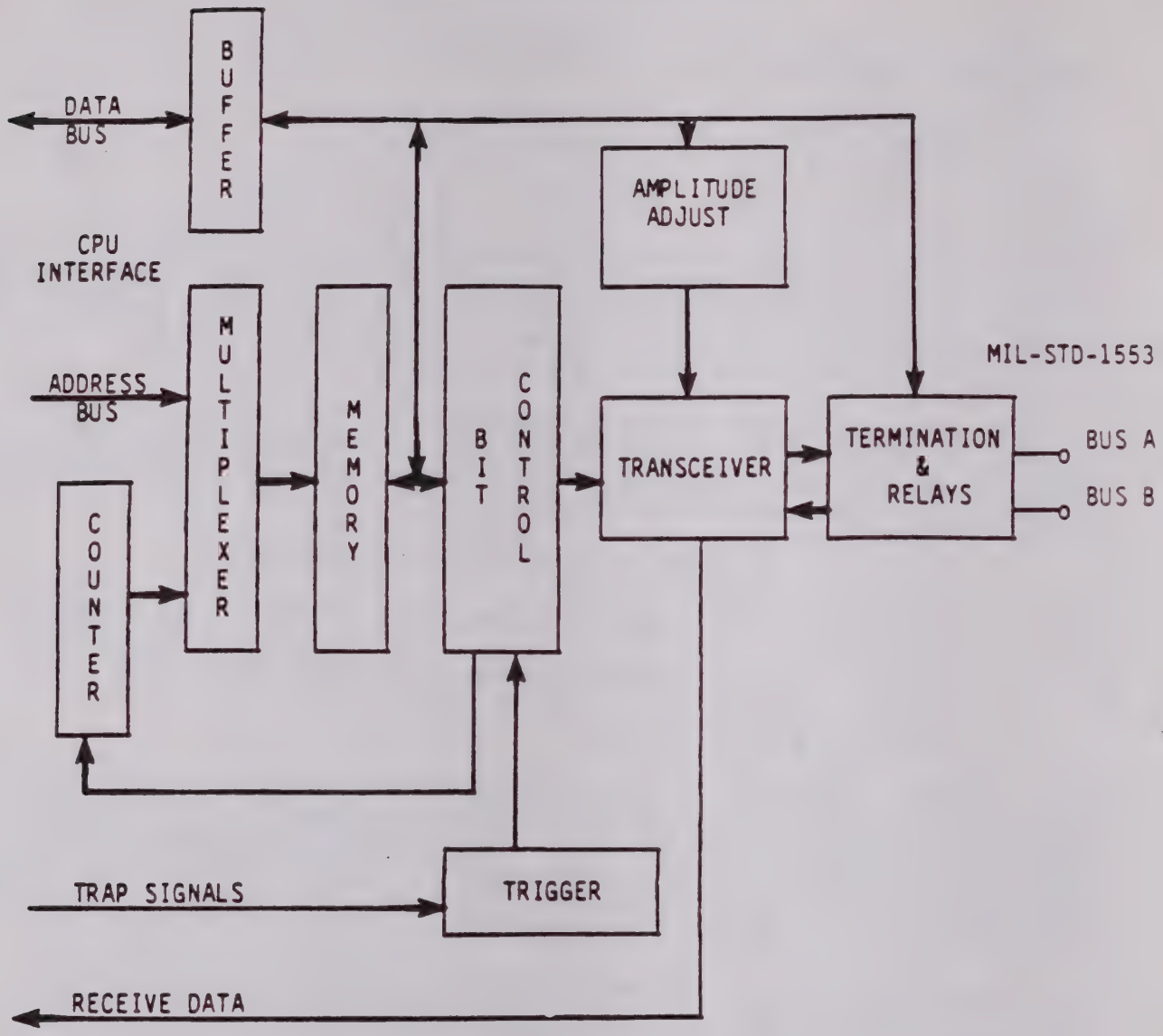
d) whether to stop the sequence.

This information feeds the Bit Control circuit which processes it and drives the transmitter portion of the transceiver. Each microsecond the bit control increments the counter to provide the address for the information describing the next microsecond in memory. The multiplexer permits both the CPU and the counter to access the memory. The memory size is 4096 bytes, so a sequence of up to 4096 microseconds, including gaps, can be defined in and transmitted by the Encoder.

The transmitted sequence may be initiated by the CPU or triggered by trap signals from the Decoder when simulating a remote terminal. The amplitude of the transmitted signal may be adjusted by varying the voltage to the transceiver. This function is provided by a power supply which may be set by the CPU. Buffering isolates the CPU Data Bus from the Encoder Data Bus.

Normally, the timing for the bit control is provided by a crystal controlled clock. When the byte from memory indicates a zero crossing variation, the crystal clock is replaced by an analog timer for one transition. The analog timer may be set by the CPU, thus providing adjustment of zero crossing time. The timer is set by the CPU before the start of the Encoder sequence. Any number of bits may have their zero crossings varied, but they are each varied by the present value.

FIGURE 6. ENCODER BLOCK DIAGRAM



## ENCODER-DETAILED CIRCUIT DESCRIPTION

Components associated with the following circuit blocks are as marked on the attached Encoder schematic:

Address Counter: While transmitting, the Address Counter points to the data in memory defining the characteristics of the next bit cell. It is kept cleared (CLKEN) until the start of an Encoder sequence when it is incremented (BITHALF) every microsecond. It can count from zero to 1023.

Address Multiplexer: The memory may be addressed by the CPU or the Address Counter. The Address Multiplexer selects between these two sources. It permits CPU access except during an Encoder sequence (CLKEN).

Memory: Each of the 1024 bytes of Memory describe the control for one microsecond of Encoder data.

Output Port Decoder: The CPU outputs to the Encoder through ports E0 to E5. The least significant port is determined by the Output Port Decoder from the CPU Address.

Memory Control: The Memory Control provides the chip select and write signals to the memory during CPU access (RAM5, WR) and during internal access (CLKEN2).

Memory Buffer: The CPU can read and write from Encoder Memory. The Memory Buffer provides isolation from the CPU Data Bus.

Bit Register: Each microsecond (bit) the data describing the next microsecond (bit) is clocked (BITHALF) into the Bit Register. Outputs of the Bit Register are as follows:

FBH = state of the first bit half
LBH = state of last bit half
XENM = transmitter enable
STOP = stop the Encoder sequence
FZC = switch in analog zero crossing time for first (mid bit) zero crossing
LZC = switch in analog zero crossing for last (at end of bit) zero crossing.

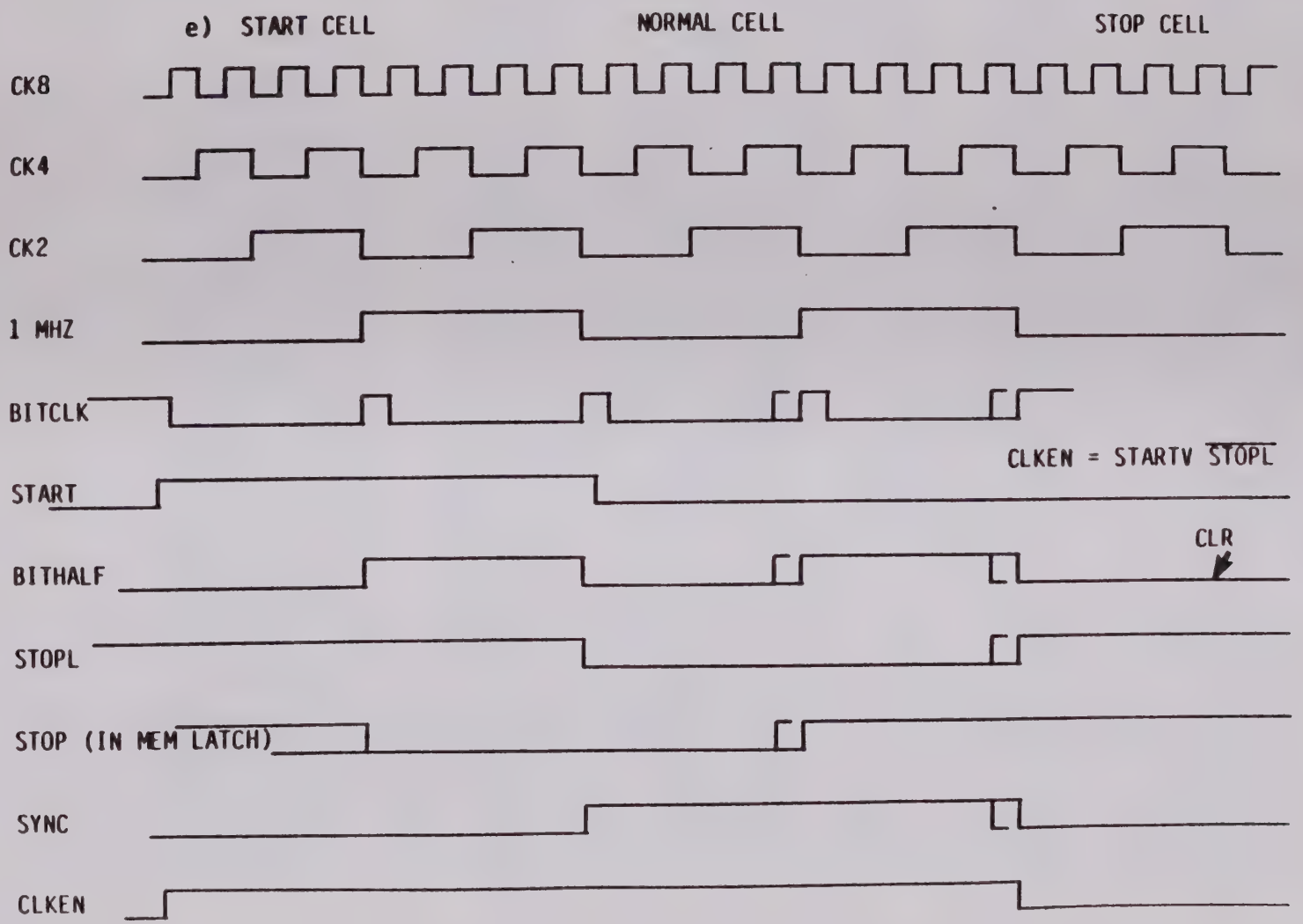
Status Buffer: The CPU can determine whether the Encoder sequence is still in progress by reading the state of STOPL through the Status Buffer at port E0.

Bit Control: Each one microsecond bit cell is divided into two halves defined by the state of BITHALF which switches the multiplexer (U9) to access the state and zero crossing information for the two halves from the Bit Register. The zero crossing signal (ZCD) is passed to Bit Timing while the Encoder polarity (ENCP) is clocked into the latch (U23) every 0.5 microsecond by BITCLK. The complementary signals (EDATA, EDATA) from the latch (U23) drive the polarity input to the transmitter in the transceiver hybrid which is enabled by the signal (XEN) from the latch (U37A). The transmitter enable signal (XENM) from the Bit Register is clocked twice each microsecond into the latch (U37A) to generate XEN. The transceiver is kept disabled except during an Encoder sequence by CLKEN on the clear of the latch (D23A).

Start/Stop: The Start/Stop circuit causes the Encoder sequence to start upon receiving an appropriate trigger and to stop when the sequence reaches a set STOP bit from the Bit Register. The start trigger may come from the trigger or (U44A) from the CPU (output port E0). The trigger causes the latch (U37B) to be set starting the Encoder sequence (CLKEN). Bit Timing generates the bit clock which is used by U23 to generate BITHALF and to latch the condition of the STOP bit from the Bit Register to create ESYNC and STOPL (see Timing in Figure 7). Once the sequence has started, start latch (U37B) is cleared (by ESYNC through U13D) and the sequence is kept enabled (CLKEN) by STOPL (inverted through U30A). When the STOP Bit in the Bit Register is set, STOPL in U23 becomes active disabling CLKEN through C23A. Since CLKEN and CLKEN are used throughout the Encoder, two inverters (U30C, U30D) are used to reduce the loading on this signal. The power on clear (POC) from the CPU is buffered (U19D, U13A) and used to initialize the Encoder. Gate C23C ensures that STOP can be latched into U23 (ESYNC, STOPL) only at the start of a bit cell. The CPU must set the STOP bit in memory at the end of an Encoder sequence or the Encoder will recycle and run continuously.

Transceiver: The transceiver is an 8559 hybrid circuit which contains both a transmitter section and a receiver section each of which are transfrormer coupled to the Termination circuit. The receiver section converts, the biphase MIL-STD-1553 signals to TTL level signals (RDATA, RDATA). This output is not truly complementary in that RDATA is active when the 1553 signal is above a certain positive threshold and RDATA is active when the 1553 signal is below a negative threshold. When the 1553 signal is between the two thresholds,

FIGURE 7. ENCODER START/STOP TIMING



neither RDATA nor RDATA is active. RDATA and RDATA are passed to the Decoder circuit board. If desired, the receiver may be disabled by the Trigger circuit (RCVEN) while the Encoder is transmitting. Complementary TTL data and enable from Bit Control are the inputs to the transmitter section. The amplitude of the transmitted signals is directly proportional to the voltage (VX) from Amplitude Adjust.

Clock: The Clock circuit is a 16 MHz crystal controlled oscillator.

Output Termination: The output termination circuitry consists of eight relays (K1-K8), a latch (U4), and four relay drivers (U2, U3, U5, U6). The various output terminations are controlled by the latch (U4) which is port E3. Diodes CR1-CR8 are used to protect the drivers from the inductive EMF when switching the relays.

Table 4 is the menu selection for the various output termination options. Table 5 is a matrix of which relay will be energized for each option.

Bit Timing: The function of Bit Timing is to generate the bit clock (BITCLK) signal twice each microsecond while the Encoder is active (CLKEN). If it was not necessary to vary the zero crossing of transmitted signals, Bit Timing would be straight forward with BITCLK occurring every 0.5 microseconds. However, any individual pulse may be made to shift by up to ±375 nanoseconds. The Bit Timing might be more correctly labeled half Bit Timing in that it generates its Timing sequence for BITCLK which occurs each half Bit Time.

The counter (U24), clocked at 16 MHz, drives the Decoder (U31) to produce the Timing pulses (C0 through C7, see Figure 8). The outputs of the counter (U24) are set when the clock is disabled (CLKEN = 0) forcing the counter to a count of zero on the first clock (CK16) after the clock is enabled (CLKEN = 1). This starts the timing in the correct state.

If no zero crossing adjustment is selected (ZCD = 1), then the zero crossing trigger enable is not be set (TREN = 0) and zero crossing delayed is not be set (ZCDF = 1), resulting in a very simple circuit (D29A, C25B, D29C, C25C, D27B). BITCLK is be clocked high by C7 = 0 on D29A feeding through to the J input of D27B. Similarly BITCLK is clocked low by C0 = 0 on D29C feeding through to the K input of D27B. This sequence will produce a BITCLK every 0.5 microsecond as shown in the normal bit in Figure 8.

TABLE 4. OPTIONS FOR 553A OUTPUT

MENU SELECTION

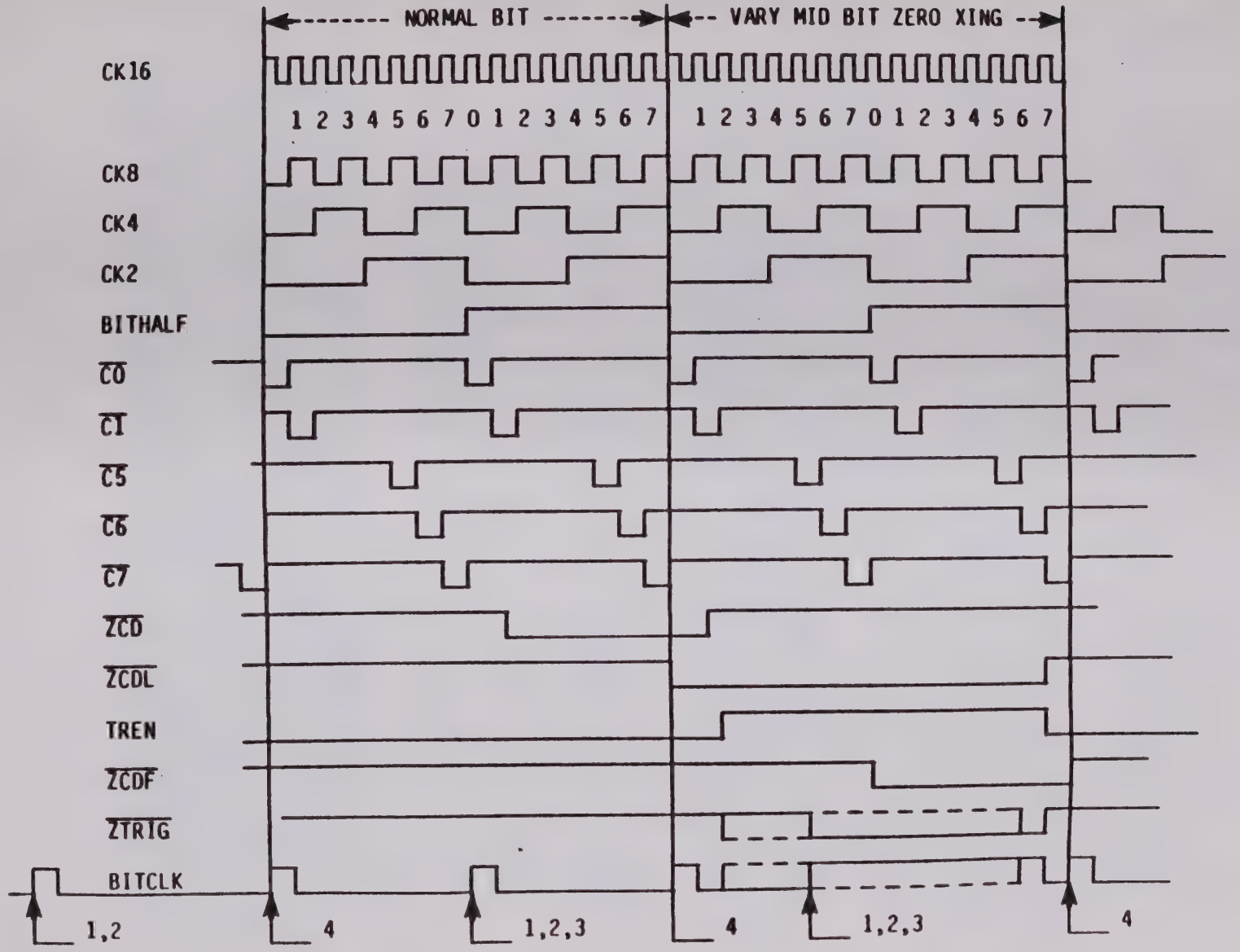
| 1553A | | 1553B | | | |
|---|---|---|---|---|---|
| Select<br>1. No<br>2. Direct<br>3. 1553A | Fig 1A | Select<br>1. No<br>2. Direct<br>3. 1553B | Fig 1B | Direct | BUS |
| Select<br>1. No<br>2. Xformer<br>3. 1553A | Fig 2A | Select<br>1. No<br>2. Xformer<br>3. 1553B | Fig 2B | Xformer | |
| Select<br>1. Yes<br>2. Direct<br>3. 1553A | Fig 3A | Select<br>1. Yes<br>2. Direct<br>3. 1553B | Fig 3B | Direct | INSTRUMENT |
| Select<br>1. Yes<br>2. Xformer<br>3. 1553A | Fig 4A | Select<br>1. Yes<br>2. Xformer<br>3. 1553B | Fig 4B | Xformer | |

## TABLE 5. RELAY MATRIX FOR ALL OPTIONS

| | SW1(K7) | SW2(K1) | SW3(K2) | SW4(K5) | SW5(K3) | SW6(K4) | SW7(K8) ON= REC CH2 / OFF = REC CH1 | | SW8(K6) ON= TX CH2 / OFF = TX CH1 | |
|---|---|---|---|---|---|---|---|---|---|---|
| FIG 1A | ON | X | X | ON | OFF | OFF | | | | |
| FIG 2A | ON | X | X | ON | OFF | OFF | | | | |
| FIG 3A & 4A | OFF | OFF | OFF | OFF | ON | OFF | | | | |
| FIG 1B | ON | X | X | ON | ON | OFF | | | | |
| FIG 2B | ON | X | X | ON | OFF | ON | | | | |
| FIG 3B | OFF | OFF | OFF | OFF | X | OFF | | | | |
| FIG 4B | OFF | ON | ON | OFF | X | OFF | | | | |

ON = LOGIC "1"
OFF = LOGIC "0"

FIGURE 8. ENCODER BIT TIMING




Action at BITCLK: 1: Latch memory data into Bit Reg; 2: Increment Address Counter;
3: Output 2nd Half; 4: Outpu st Half.

When the zero crossing adjust is selected (ZCD = 0) for a bit half, it is the zero crossing at the end of the bit half which gets varied. ZCD gets latched into U46B and U46A in the correct timing by gating (U39D, U39C) with Timing Signals to create the zero crossing timer enable (TREN). The bit clock (BITCLK, U25A) is set by the analog timer (ZTRIG) from the Zero Crossing Adjust circuit. BITCLK is cleared by Timing Signals C6 and ZCDF (U32, U25A) in time for the next normal BITCLK. If for some reason the analog timer has not set BITCLK by the end of the bit (+375 nS from normal), then BITCLK is set by the Timing Signals C5 and ZCDF (U32A, U19C, U25A). This guarantees a BITCLK before the next normal BITCLK. The remaining gates and flip flop (U39A, U39B, U25B, U32C) generate additional Timing Signals (ZCDF, TRR).

Amplitude Adjust: The amplitude of the transmitted 1553 signal is directly proportional to output voltage (VX) from the Amplitude Adjust circuit. The CPU can set the voltage (VX) between zero and +15 volts DC. The digital setting for the voltage is loaded by the CPU into the register (U10) by an output to port E4. This setting is then applied to the input of the digital to analog converter (DAC, U11). The DAC sinks a current at its output (XW1) which is directly proportional to its digital setting and the reference current (XW8). The reference current is the 7.1 volt reference voltage (U7) divided by the sum of the 3K resistor and the 1K potentiometer setting in the XW7, XW2, XW8 circuit. Normal reference current is about 2 mA (7.1/3K+550). The amplifier (U7, T7P120) Q1 is basically a current to voltage converter. At full scale, the DAC sinks 2 mA at XW1. The output voltage (VX) is the DAC current times the 7.5K ohm feedback resistor. The 16 volt zener helps protect the transceiver from excess voltage should there be a failure in the DAC or amplifier. The 1K potentiometer is used to calibrate the output for +15 volts DC at full scale (FA in U10). The small capacitors (100 pF and 20 pF) stabilize the circuit. The two 1K resistors (R15, R16) are a voltage divider to bias the zener reference (U7).

Zero Crossing Adjust: The Zero Crossing Adjust circuit is the analog timer which the Bit Timing uses to shift the bit clock. The register (U14) latches the digital value (ZB0 through ZB7) from a CPU output to port E5 and provides the digital value for the digital to analog converter (DAC, U15) which sinks a current at ZW1 proportional to the digital input and the reference circuit. The 2.5 volt zener (LM336) and the 1.2K resistor set the reference current to about 2 mA ($I_{REF}$=2.5/1.2K). The operational amplifier (U16) converts the current into the DAC at ZW1 to a positive voltage at ZW5. The positive (+) input of the op amp comes from the potentiometer tap (R2) in a

resistor divider circuit which is used to shift the output (ZW5) of the op amp. The gain of the op amp is adjusted by the potentiometer (R28). The resulting output voltage is:

$$V_{ZW5} = I_{DAC} (1.2K + R1) - V_{ZW3}$$

Remember that $I_{DAC}$ is a function of the digital input, so for any fixed digital input there is a fixed $V_{ZW5}$. R28 and R19 are used only for calibration.

The transistor (2N2907) is a current source feeding the 0.0022 uF capacitor (i.e. a linear ramp generator). The capacitor is discharged through the 10 ohm current limiting resistor by the driver (U12) to ground. The timer enable signal (TREN) from the Bit Timing turns the driver off enabling the capacitor voltage (ZW8) to ramp up. The DAC amplifier voltage (ZW5) and the ramp voltage (ZW8) are compared (U17) to give an output (ZTRIG) proportional in time to the setting of the DAC. After being enabled by TREN, the ZW8 voltage increases and when it becomes greater than the ZW5 voltage, the comparator switches (ZTRIG=0). See Figure 9 for waveforms.

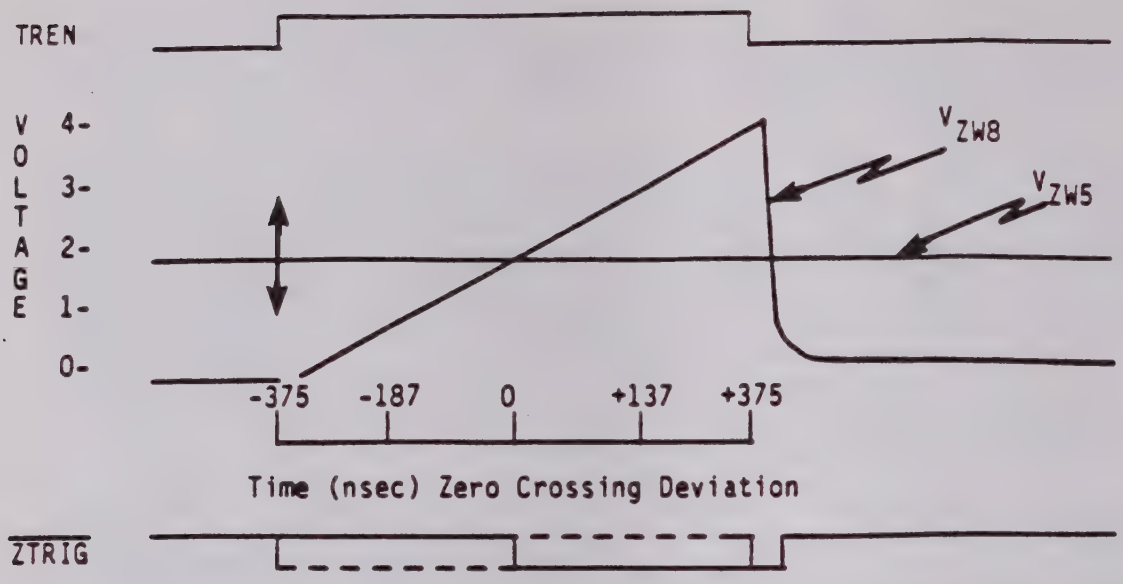
Associate Interface: Beside the MIL-STD-1553 Buses three signals interface to the back panel of the Model 553 via J4. An external trigger is applied to J4 pin 10. The diodes and resistor protect the gate (U45C) from excess voltage. The two outputs, Encoder sync (J4 pin 6) and trap pulse (J4 pin 2), are buffered by the 50 ohm line driver (U40).

Trigger: Various trigger and control functions are accomplished by the Trigger circuit. the options are selected by the CPU outputting to the register (U33) at port E2. Four functions are set by this register:

1) RT Mode (RTMODE)
2) External Trigger Select (XTRGSEL)
3) Fast Repeat (FASTRPD)
4) Display Receive Only (DISPRO).

The output (TRGR) of the flip flop (U38B) starts the Encoder sequence on each falling edge. When simulating an RT (RTMODE = 1), the flip flop (U38A) is armed (i.e. set) when a trap pulse (TRAPP) is received from the Decoder. Then when a very dead line (VDL) is detected by the Decoder, the signal propagates through the gates (U45A, R45B) to the flip flop (U38B) which starts (TRGR) the Encoder sequence. When external trigger (XTRGSEL) is selected, the gates (U45C, U45B) permit the external trigger (XTRIG) from the Associate Interface to start the Encoder by clocking the flip flop (U38B). In order for the flip flop (U38B) to trigger again it must be cleared. When fast repeat

FIGURE 9. TIMING OF ZERO CROSSING ADJUST SHOWN WITH $V_{ZW5}$ SET FOR 0 DEVIATION

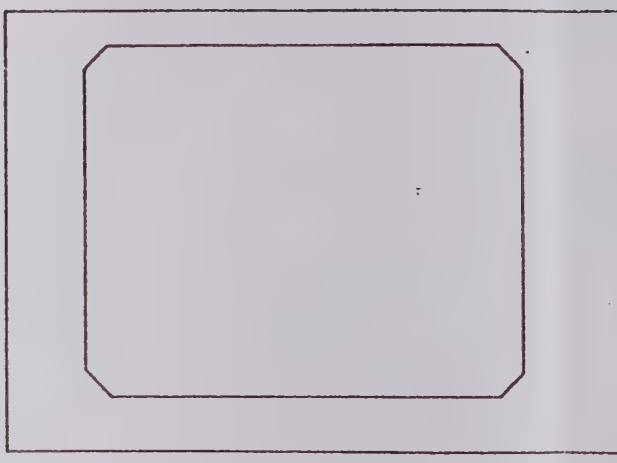


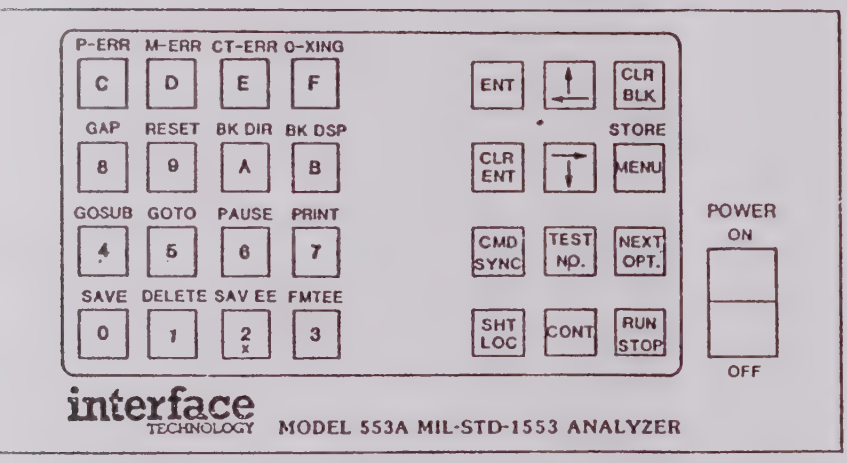
(FASTRPT) is selected, this clearing is accomplished by the Encoder sequence itself (ESYNC) through the gates (U44C, U13B). Otherwise, it may be cleared through gates (U18B, U13B) by a power on clear (POCL) or a CPU output to port E1. To prevent the Decoder from trapping on data transmitted by the Encoder in RT Mode, the Decoder Trap is disabled (TRAPD) by the gated (U44B) combination of RTMODE and the Encoder clock enable (CLKEN). The Decoder may be totally disabled (not able to receive) while the Encoder is transmitting by gating (U30B) DISPRO with the Encoder clock enable (CLKEN).

# APPENDIX H. SCHEMATICS

The following schematics and logic diagrams are included herein:

| | |
|---|---|
| 20010001 | Front Panel Illustration |
| 20010060 | Rear Panel Illustration |
| 20011604 | Decoder |
| 20010004 | Encoder |
| 20010016 | CPU |
| 20010012 | User Board |
| 20010008 | Sine/Trap (Optional) |






| QTY REQD | FSCM NO. | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | MATERIAL SPECIFICATION |
|---|---|---|---|---|

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±

CONTRACT NO.

| APPROVALS | DATE |
|---|---|
| DRAWN KAR | |
| CHECKED | |
| ISSUED | |

MATERIAL

FINISH

DO NOT SCALE DRAWING

| NEXT ASSY | USED ON |
|---|---|
| | 553A |

APPLICATION

interface TECHNOLOGY
A Dynatem Company
150 East Arrow Highway
San Dimas, CA 91773

FRONT PANEL

| SIZE | FSCM NO | DWG NO. | REV |
|---|---|---|---|
| D | | 20010001-ILLUST | |

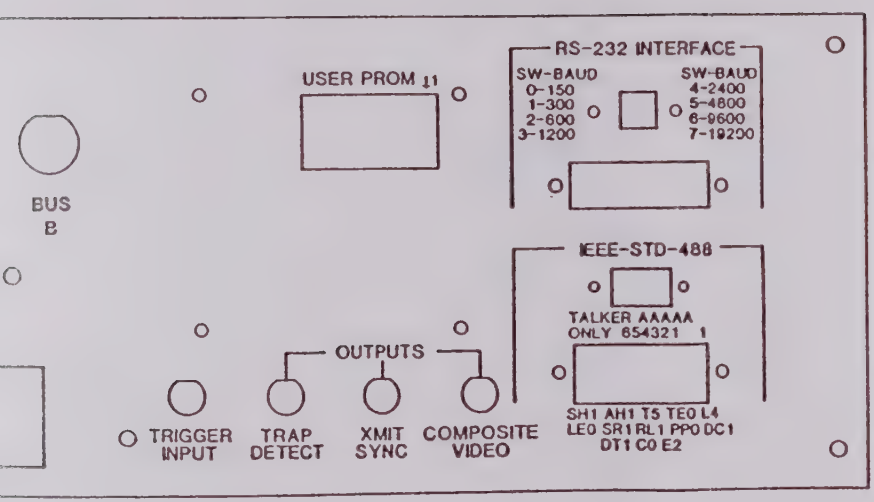
SCALE SHEET

4 3 2 1

D C B A

SINE
TRAP
BUS
A

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPROVED |




| QTY REQD | FSCM NO. | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | MATERIAL SPECIFICATION |
|---|---|---|---|---|
| PARTS LIST | | | | |

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

CONTRACT NO

| APPROVALS | DATE |
|---|---|
| DRAWN KAR | |
| CHECKED | |
| ISSUED | |

MATERIAL

FINISH

DO NOT SCALE DRAWING

553A

NEXT ASSY | USED ON

APPLICATION

interface TECHNOLOGY
A Dynatech Company
150 East Arrow Highway
San Dimas CA 91773

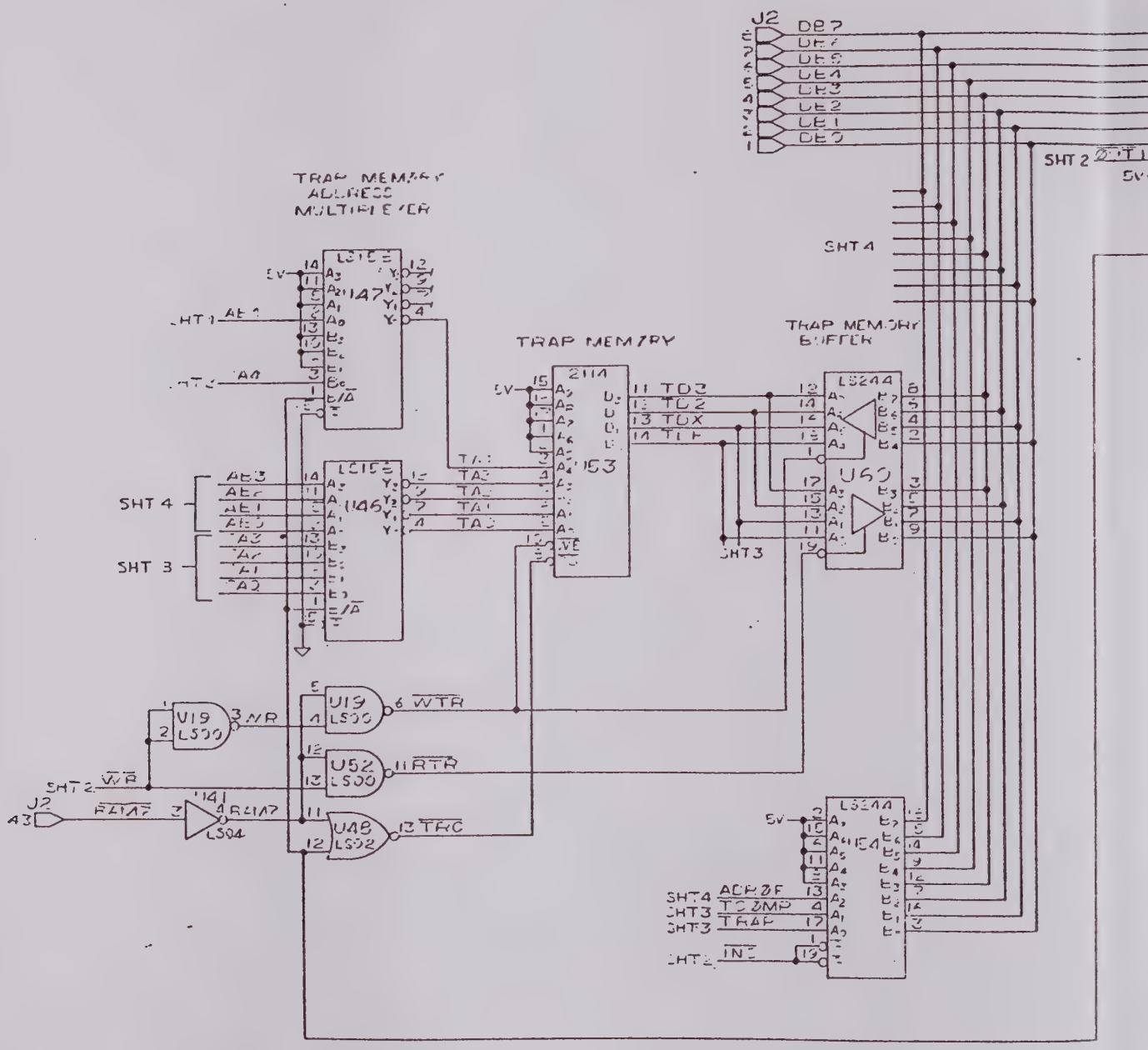
REAR · PANEL

| SIZE | FSCM NO. | DWG NO. | REV |
|---|---|---|---|
| D | | 20010060-ILLUST | |

SCALE | SHEET

NOTES: UNLESS OTHERWISE SPECIFIED

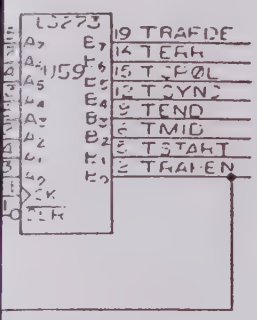
1. REFERENCE CIRCUIT CARD ASSY NO. 10011602.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 50V.



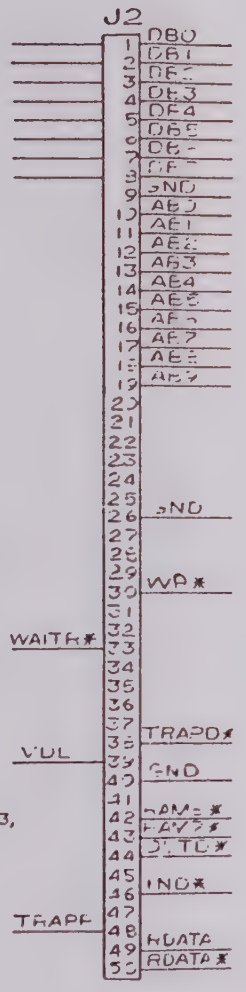

| | |
|---|---|
| Y1 | — |
| U63 | — |
| J2 | — |
| C36 | — |
| LAST USED | NOT USED |
| REFERENCE | DESIGNATIONS |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APPR | DESC. |
| – | 3-1-84 | | PRODUCTION RELEASE |

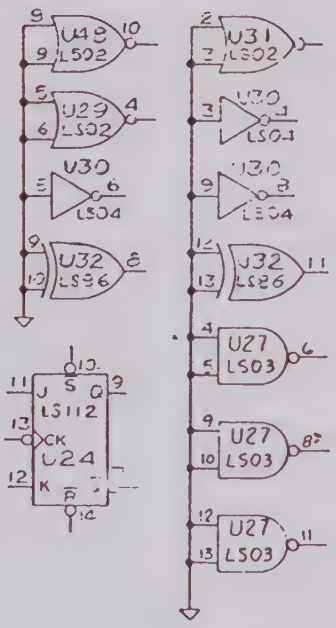
TRAP CONTROL

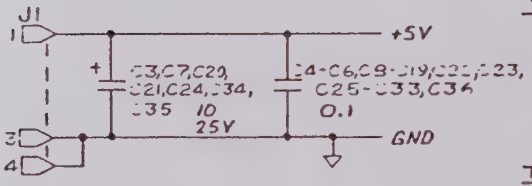



SHT 3




SPARES



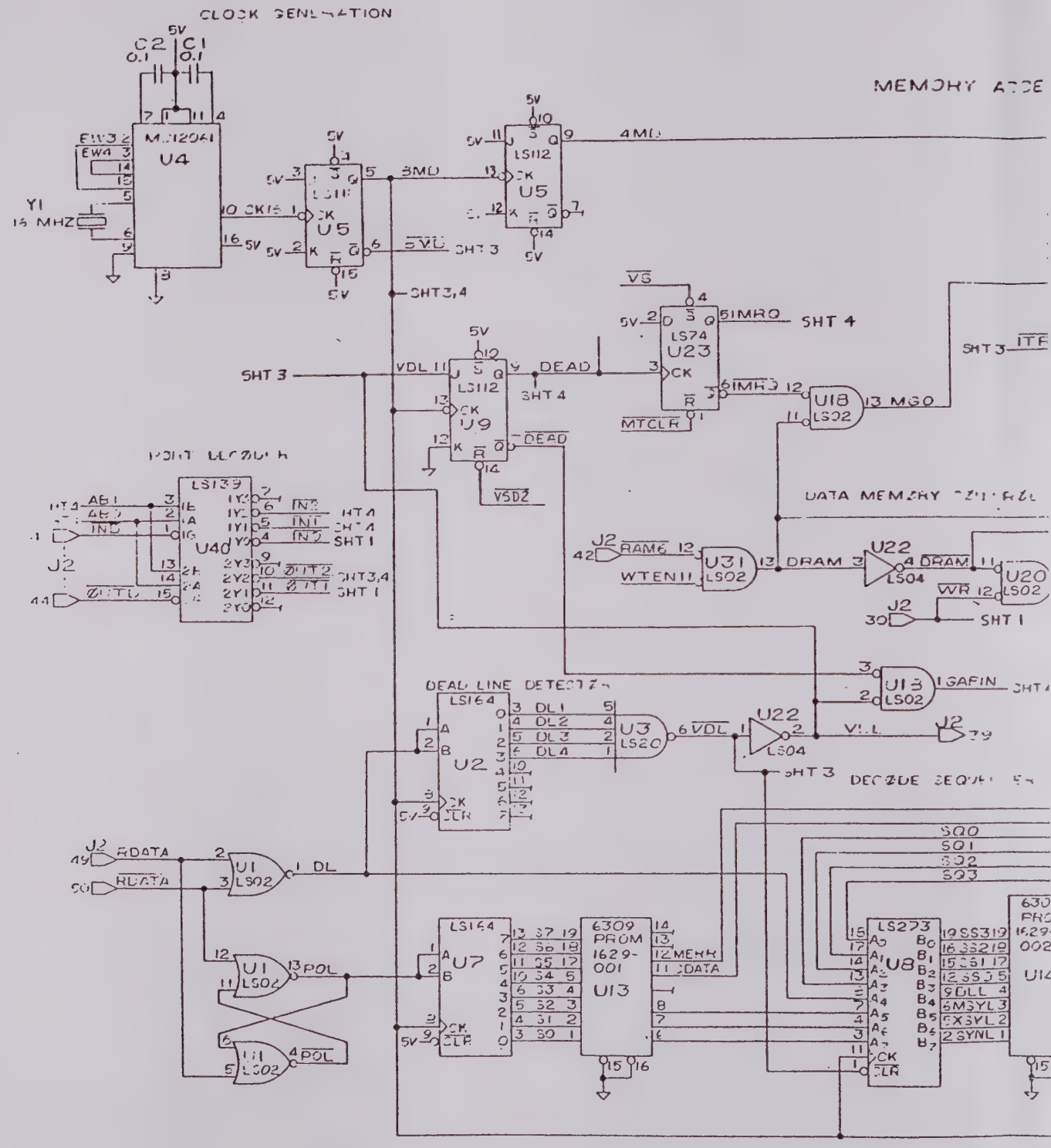

| | |
|---|---|
| 10011602 | MODEL 553 |
| NEXT ASSY | USED ON |
| APPLICATION | |

interface TECHNOLOGY

| | | |
|---|---|---|
| SCALE: NONE | APPROVED BY: MEK | DRAWN BY: J.B. |
| DATE: 11-28-83 | | REVISED |

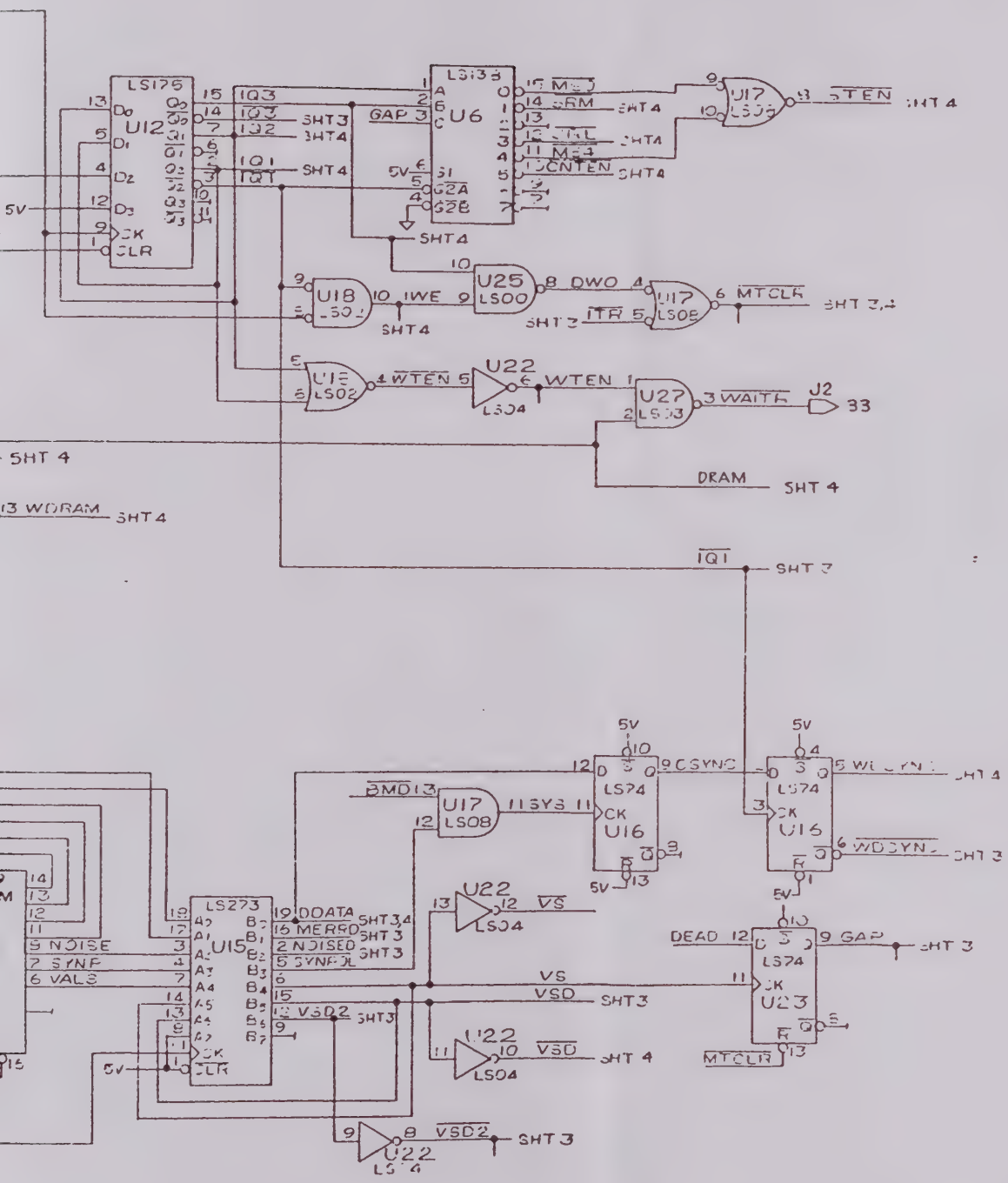
LOGIC DIAGRAM - DECODER

| | | |
|---|---|---|
| SHT. 1 OF 4 | 55613 | 10011604 |

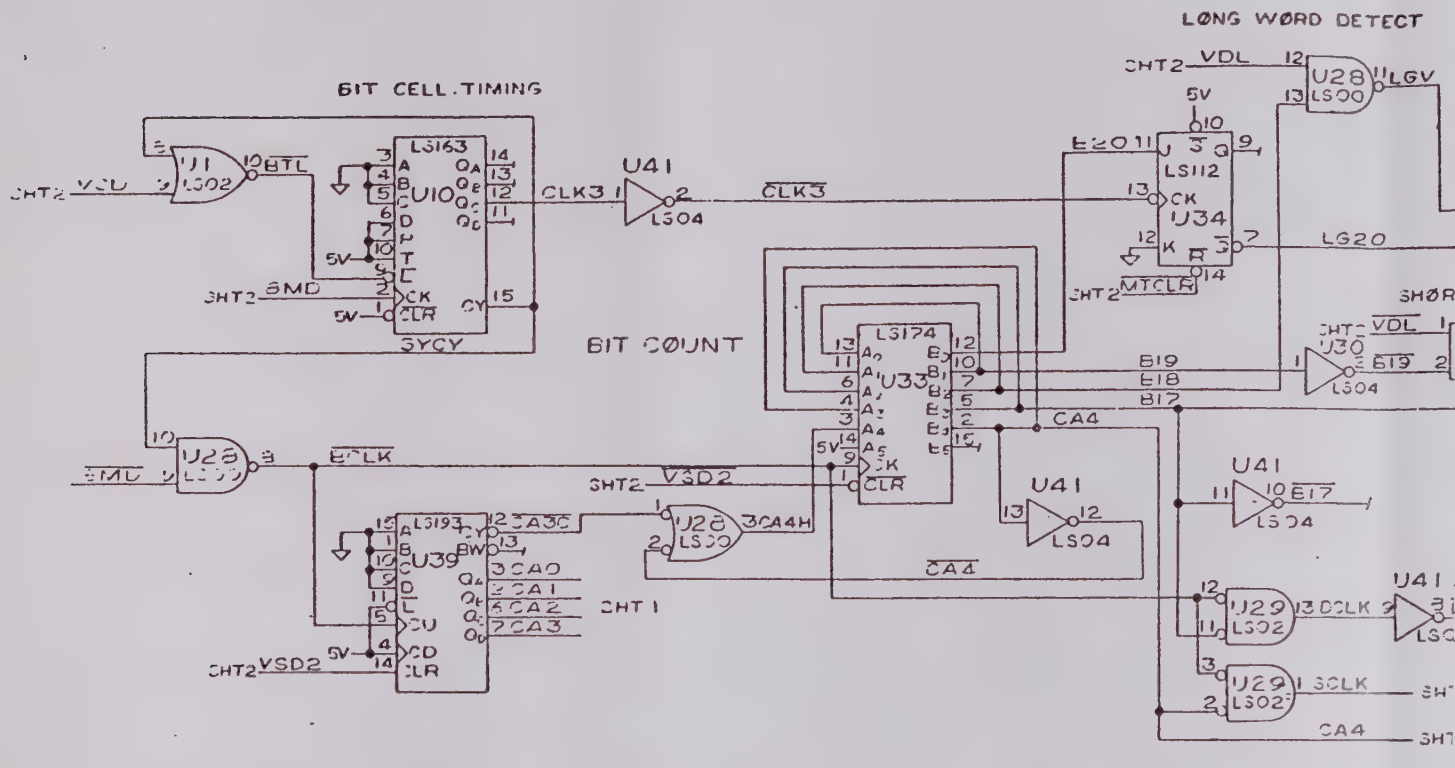

CLOCK GENERATION
MEMORY ACCE
C2 0.1
C1 0.1
5V
U4
Y1
15 MHZ
U5
LS112
4MD
3MD
SHT 3
SHT 3,4
VS
LS74
U23
SIMRQ
SHT 4
IMRQ
U18
LS02
MGO
MTCLR
SHT 3
VDL
DEAD
U9
VSDZ
POINT DECODER
LS139
U4d
IN3
IN1
IN2
SHT A
SHT 1
J2
DATA MEMORY CONTROL
RAMG
WTEN
U31
DRAM
U22
LS04
U20
WR
DEAD LINE DETECTOR
LS164
U2
DL1
DL2
DL3
DL4
U3
LS20
VDL
GAFIN
U13
DECODE SEQUENCE
RDATA
RLATA
U1
DL
POL
U7
6309
PROM
1629-
001
MEMRR
CDATA
LS273
U8
SQ0
SQ1
SQ2
SQ3
SS3
SS2
SS1
DLL
MSYL
XSYL
SYNL

| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APPR | DESC. |
| | | | SEE SHT. 1 |

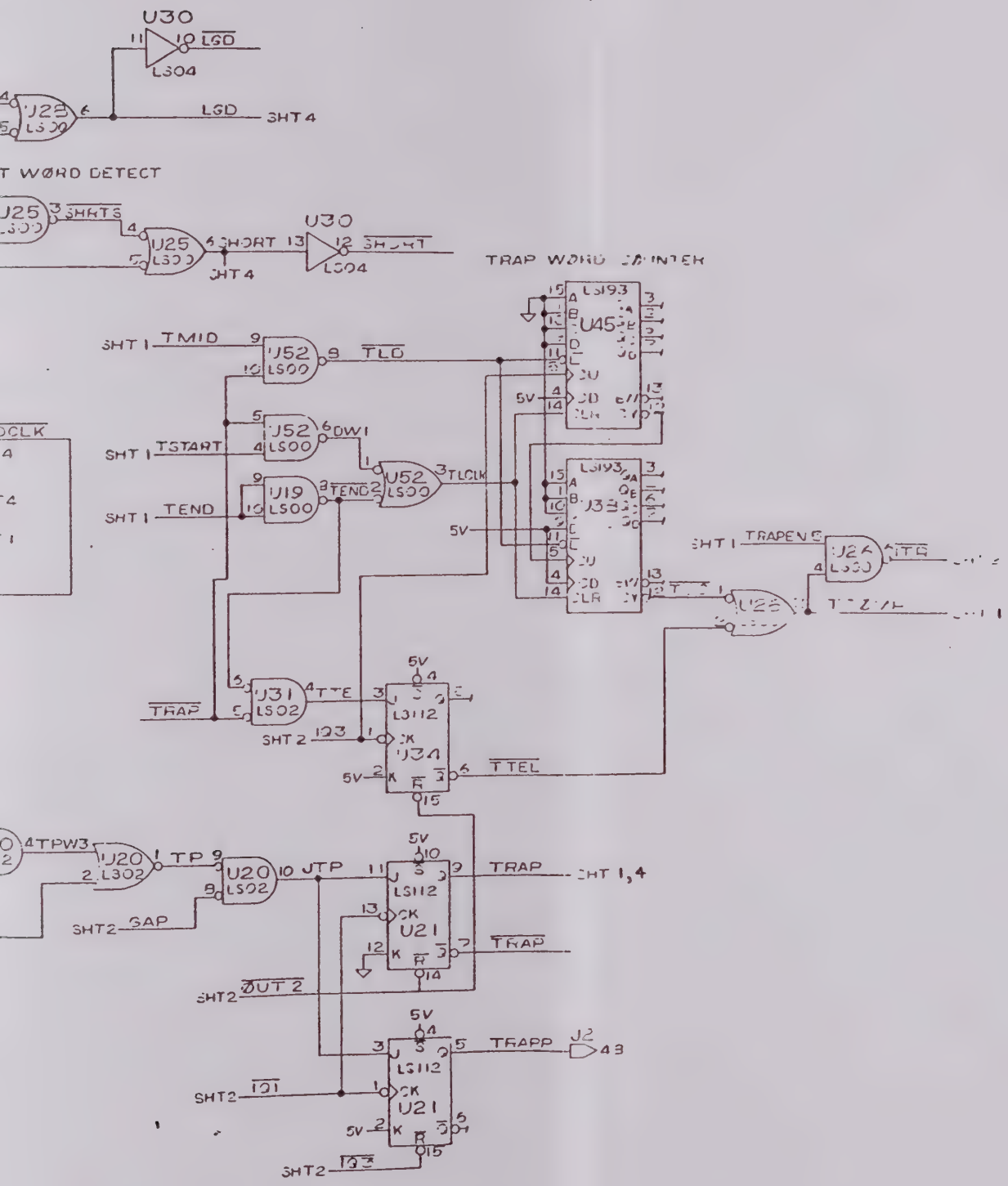
SC TIMING



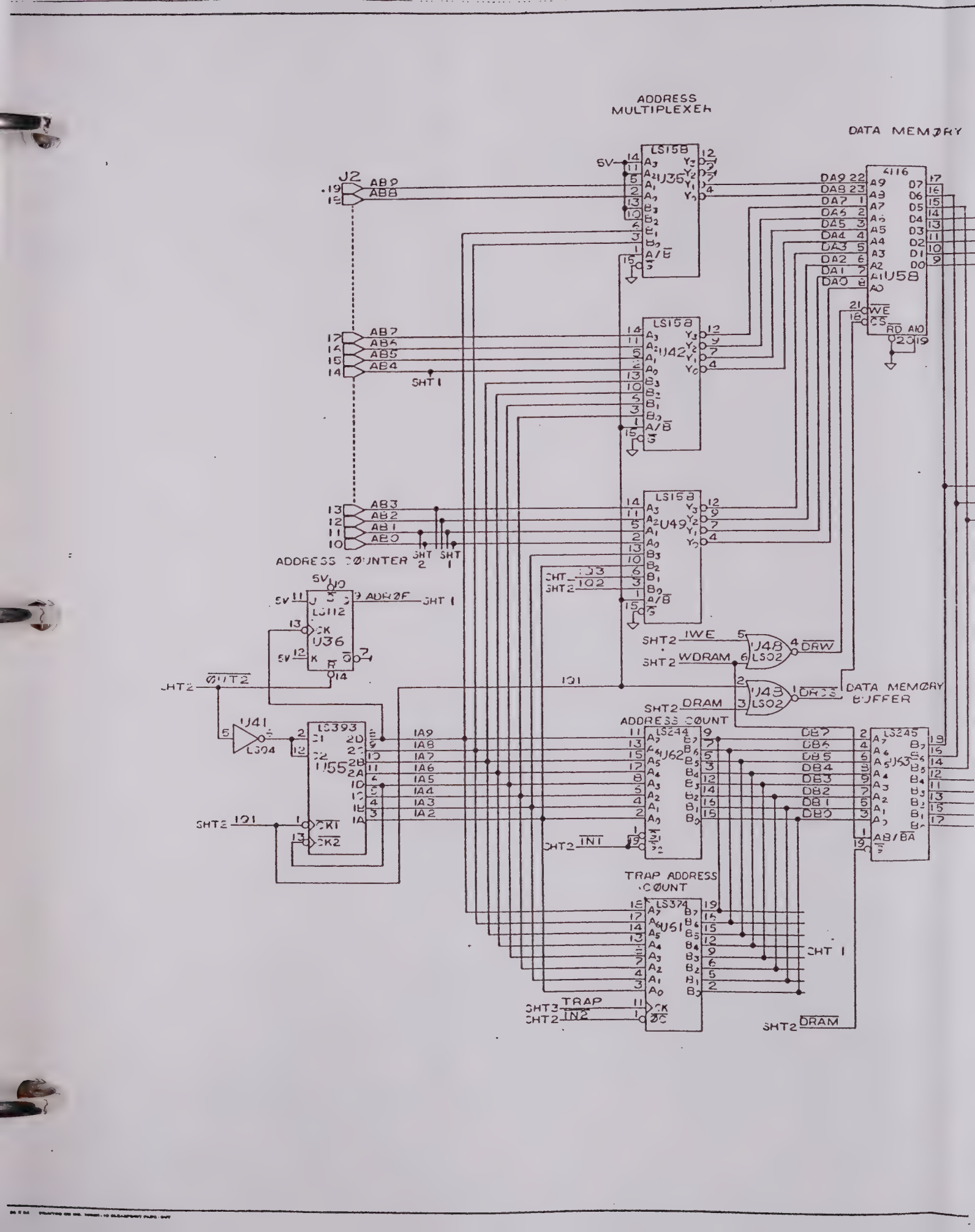

| interface TECHNOLOGY | | |
|---|---|---|
| SCALE: NONE | APPROVED BY: | DRAWN BY |
| DATE: | | DESIGNED |
| LOGIC DIAGRAM - DECODER | | |
| SHT. 2 | 55613 | DRAWING NUMBER 10011604 |


BIT CELL TIMING
LONG WORD DETECT
BIT COUNT
SHORT
U11
LS502
BTL
LS163
U10
CLK3
U41
LS04
LS112
U34
LG20
MTCLR
LS174
U33
B19
B18
B17
CA4
LS193
U39
CA0
CA1
CA2
CA3
CA4H
CA3C
CHT1
VSD2
EMD
ECLK
U28
LS00
U29
LS02
DCLK
SCLK
U30
LS04
TRAP DETECT
DLATA
DCLK
U9
PARERR
MERRD
MERRL
PERR
SHORT
LGD
U3
LS20
ERR
TERRI
U26
TPE
U19
TPE
WDSYNC
TSPOL
U32
LS86
TSC
U31
TSYNC
TSCG
TDP
TDC
TDX
U17
LS09
JTD
J2
TRAPD
U24
BTRAP
TRAPDE
NOISED
NOISEL
SHT1
SHT2
SHT4
5V

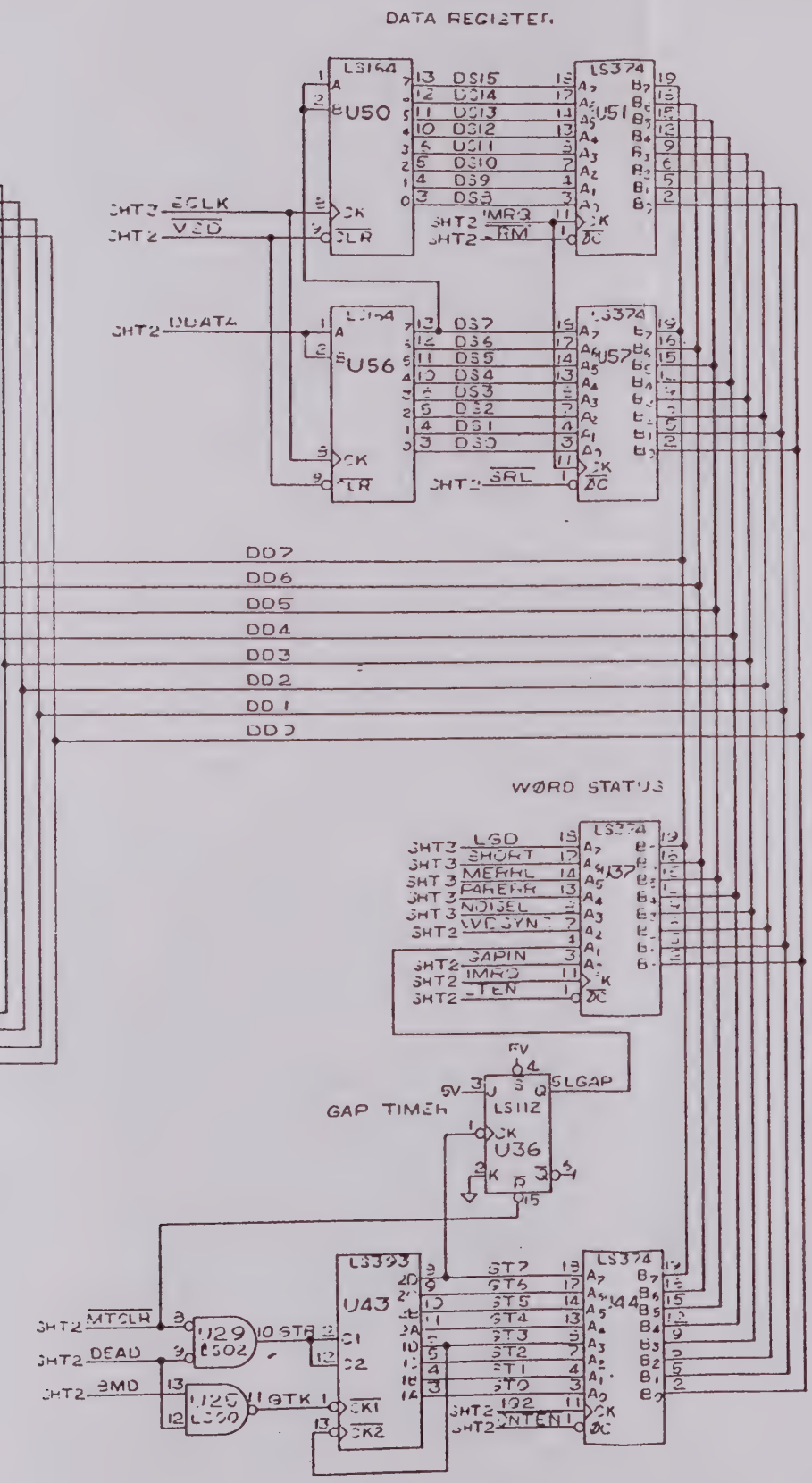
| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APPR | DESC. |
| | | | SEE SHT. 1 |




| interface TECHNOLOGY | | |
|---|---|---|
| SCALE: NONE | APPROVED BY: | DRAWN BY |
| DATE: | | REVISED |
| LOGIC DIAGRAM - DECODER | | |
| SHT. 3 | 55613 | DRAWING NUMBER 10011604 |


ADDRESS MULTIPLEXER
DATA MEMORY
J2
AB9
AB8
AB7
AB6
AB5
AB4
AB3
AB2
AB1
AB0
ADDRESS COUNTER
SHT 1
SHT 2
5V
LS158
U35
U42
U49
A/B
G
4116
U58
DA9
DA8
DA7
DA6
DA5
DA4
DA3
DA2
DA1
DA0
WE
CS
RD
A10
LS112
U36
ADR0F
SHT 1
SHT2
WRT2
U41
LS04
LS393
U55
1A9
1A8
1A7
1A6
1A5
1A4
1A3
1A2
CK1
CK2
121
131
IWE
WDRAM
DRAM
U48
LS02
DRW
U43
DRDB
DATA MEMORY BUFFER
ADDRESS COUNT
LS244
U62
INT
LS245
U63
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
AB/BA
TRAP ADDRESS COUNT
LS374
U51
TRAP
IN2
SHT3
CHT 1
CHT2
DRAM

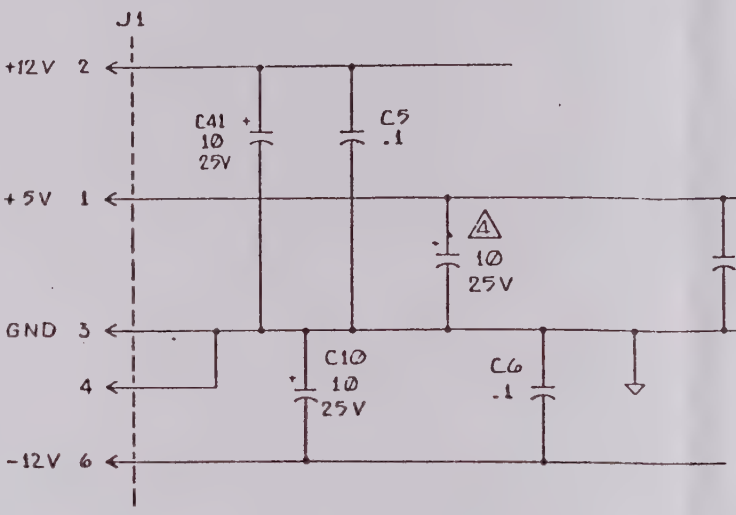
| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APPR | DESC |
| | | | SEE SHT 1 |



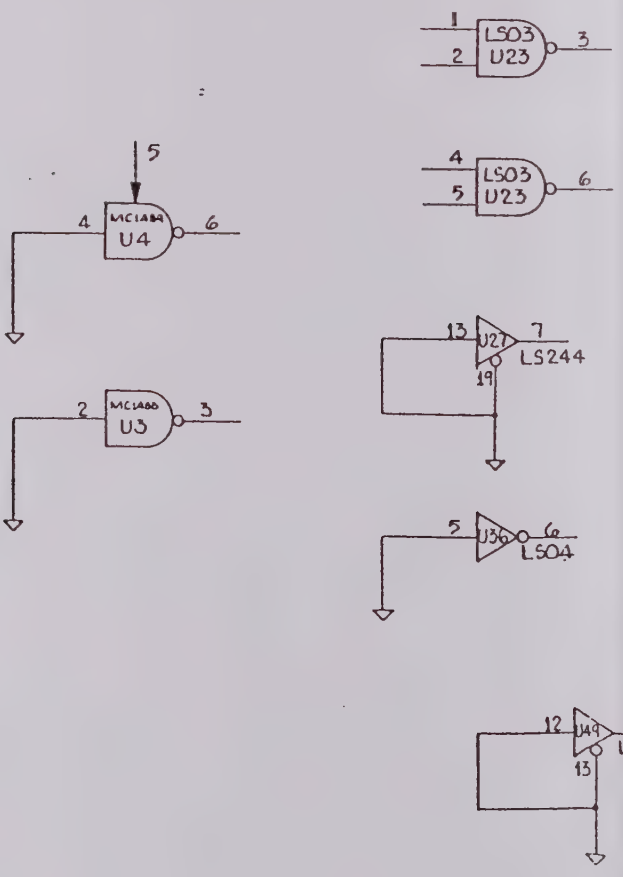

| interface TECHNOLOGY | | | |
|---|---|---|---|
| SCALE: NONE | APPROVED BY: | DRAWN BY | |
| DATE: | | REVISED | |
| LOGIC DIAGRAM - DECODER | | | |
| SHT. 4 | 55613 | DRAWING NUMBER 10011604 | |

NOTES: UNLESS OTHERWISE SPECIFIED.

1. REFERENCE: CIRCUIT CARD ASSY * 20010014.
2. RESISTANCE VALUES ARE IN OHMS, 1/8 W. ± 5%
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 50 V.
4. TYPICAL: C2, C3, C17, C18, C24, C26, C28.
5. TYPICAL: C1, C4, C9, C11, C12, C14 - C16, C19 - C23, C27, C34, C35, C38, C40.
6. SUPPLY PINS ON U18 AND U22 ARE AS FOLLOWS:
   PIN 14 — +5V
   PIN 7 — GND

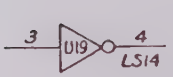


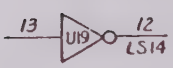

SPARES




| | |
|---|---|
| Y2 | — |
| U53 | U26, U31 |
| TP2 | — |
| R17 | — |
| Q2 | — |
| J8 | — |
| CR1 | — |
| C41 | — |
| LAST USED | NOT USED |
| REFERENCE DESIGNATIONS | |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APPR | DESC. |
| 10 | 6 6 85 | | PRODUCTION RELEASE |
| A | 7 3 85 | | CHANGE PARTS & ADD REF. |
| | | | |
| | | | |




| | |
|---|---|
| 20010014 | MODEL 553A |
| NEXT ASSY | USED ON |
| APPLICATION | |

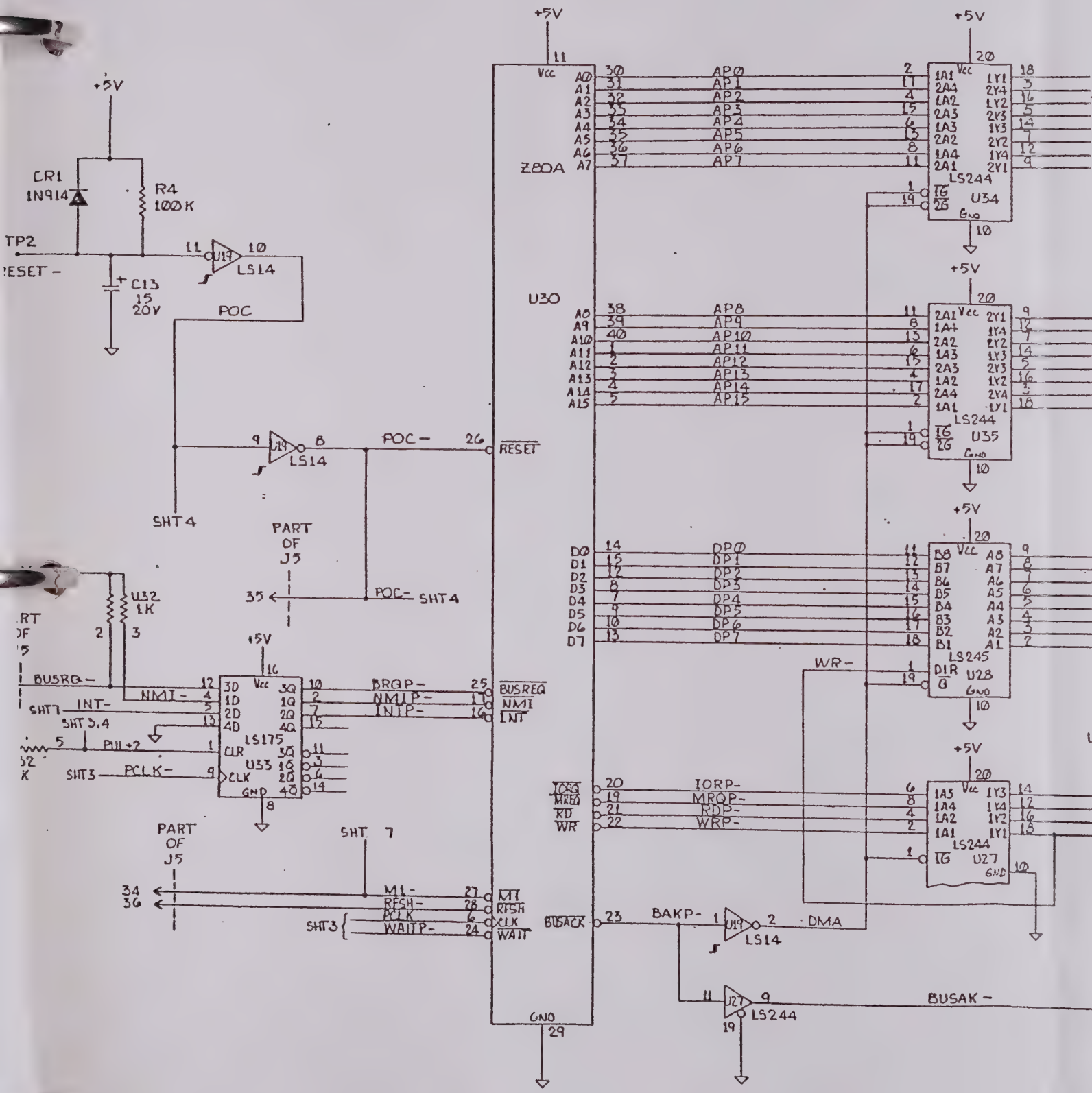
**interface** TECHNOLOGY

| | | |
|---|---|---|
| SCALE NONE | APPROVED BY: | DRAWN BY KAR |
| DATE 6-6-85 | | REVISED |

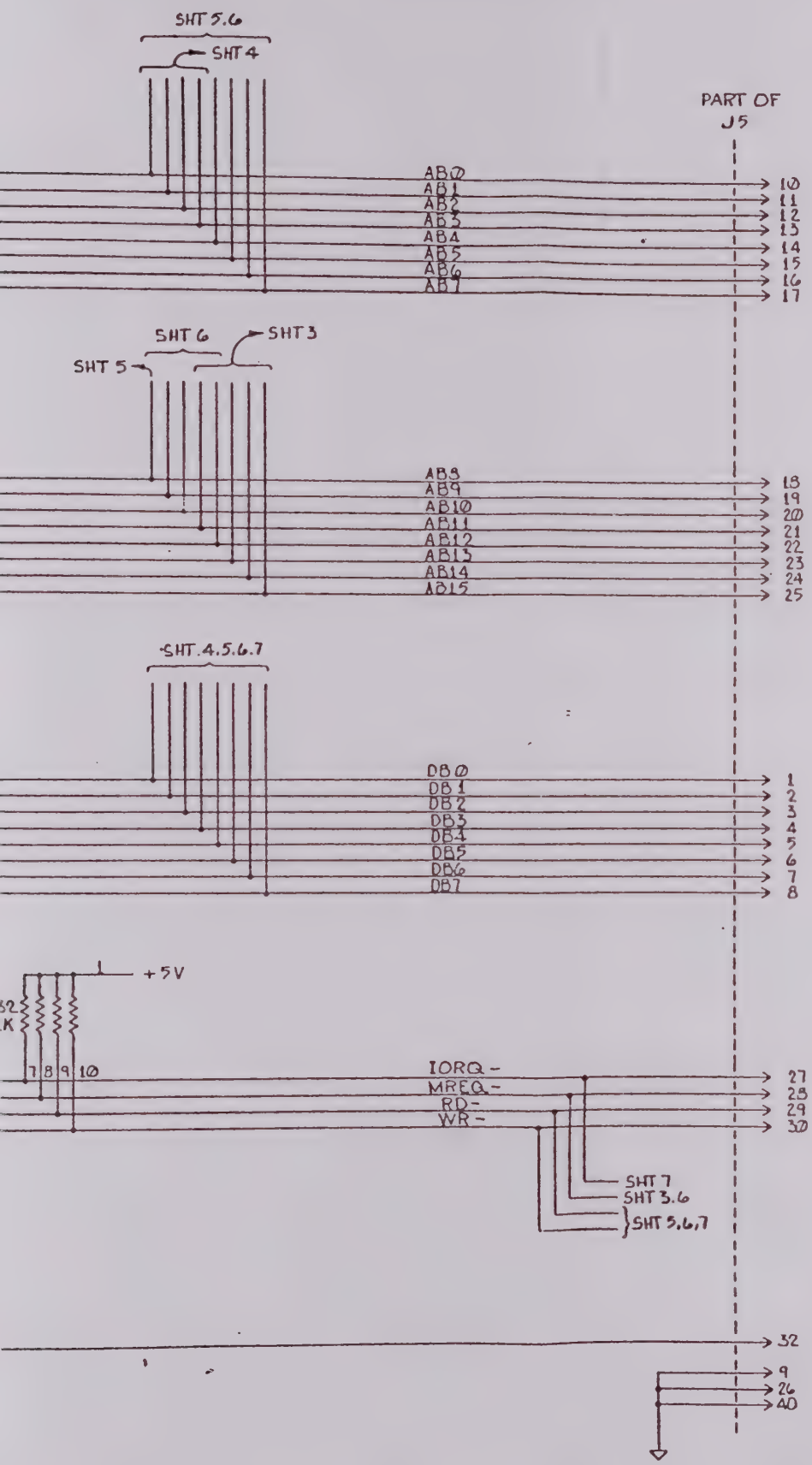
SCHEMATIC - CPU

| | | | |
|---|---|---|---|
| SHT 1 OF 7 | 55613 | REV A | DRAWING NUMBER 20010016 |

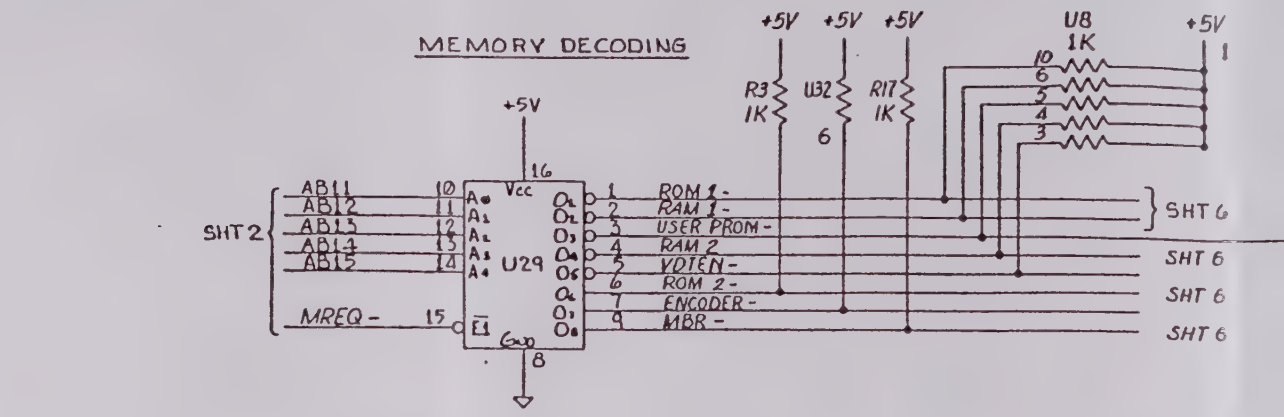
# CPU

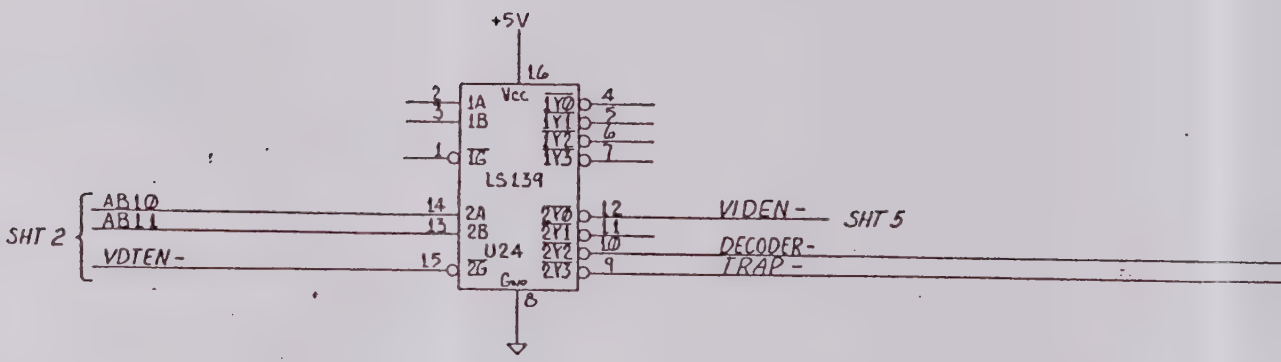

+5V
CR1
1N914
R4
100K
TP2
RESET-
U19
LS14
C13
15
20V
POC
SHT4
POC-
RESET
PART
OF
J5
35
SHT4
U32
1K
BUSRQ-
NMI-
INT-
SHT7
SHT 5,4
PHI+2
SHT3
PCLK-
LS175
U33
BRQP-
NMIP-
INTP-
BUSREQ
NMI
INT
SHT 7
34
36
M1-
RFSH-
PCLK
WAITP-
M1
RFSH
CLK
WAIT
Z80A
U30
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AP0
AP1
AP2
AP3
AP4
AP5
AP6
AP7
A8
A9
A10
A11
A12
A13
A14
A15
AP8
AP9
AP10
AP11
AP12
AP13
AP14
AP15
DP0
DP1
DP2
DP3
DP4
DP5
DP6
DP7
LS244
U34
U35
U27
LS245
U28
DIR
WR-
IORQ
MREQ
RD
WR
IORP-
MRQP-
RDP-
WRP-
BUSACK
BAKP-
DMA
BUSAK-
GND

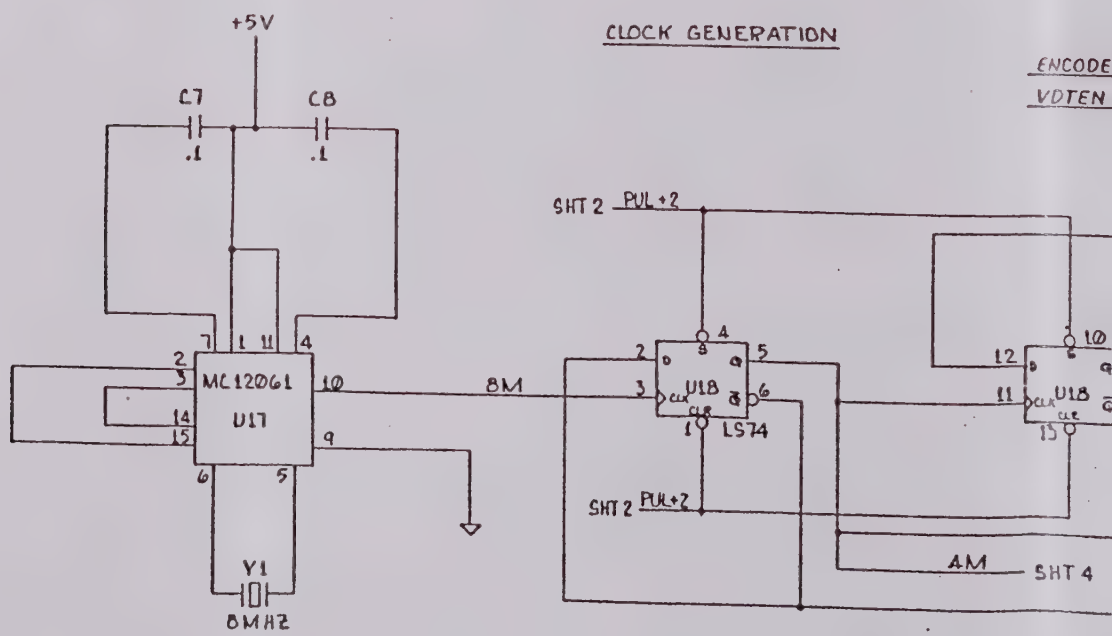
| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APPR | DES |
| IS | | | SEE SHEET 1 |
| A | | | SEE SHEET 1 |

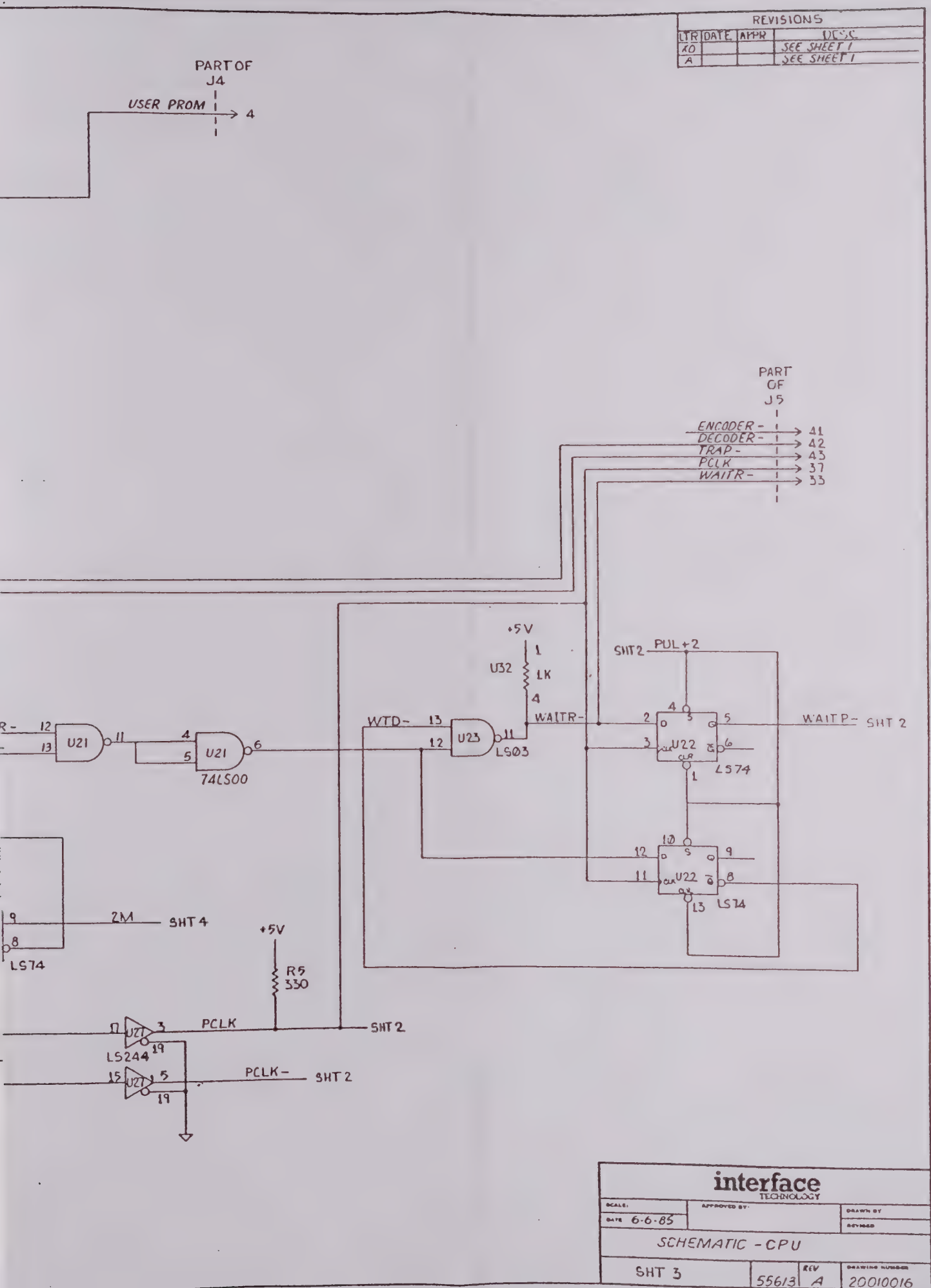


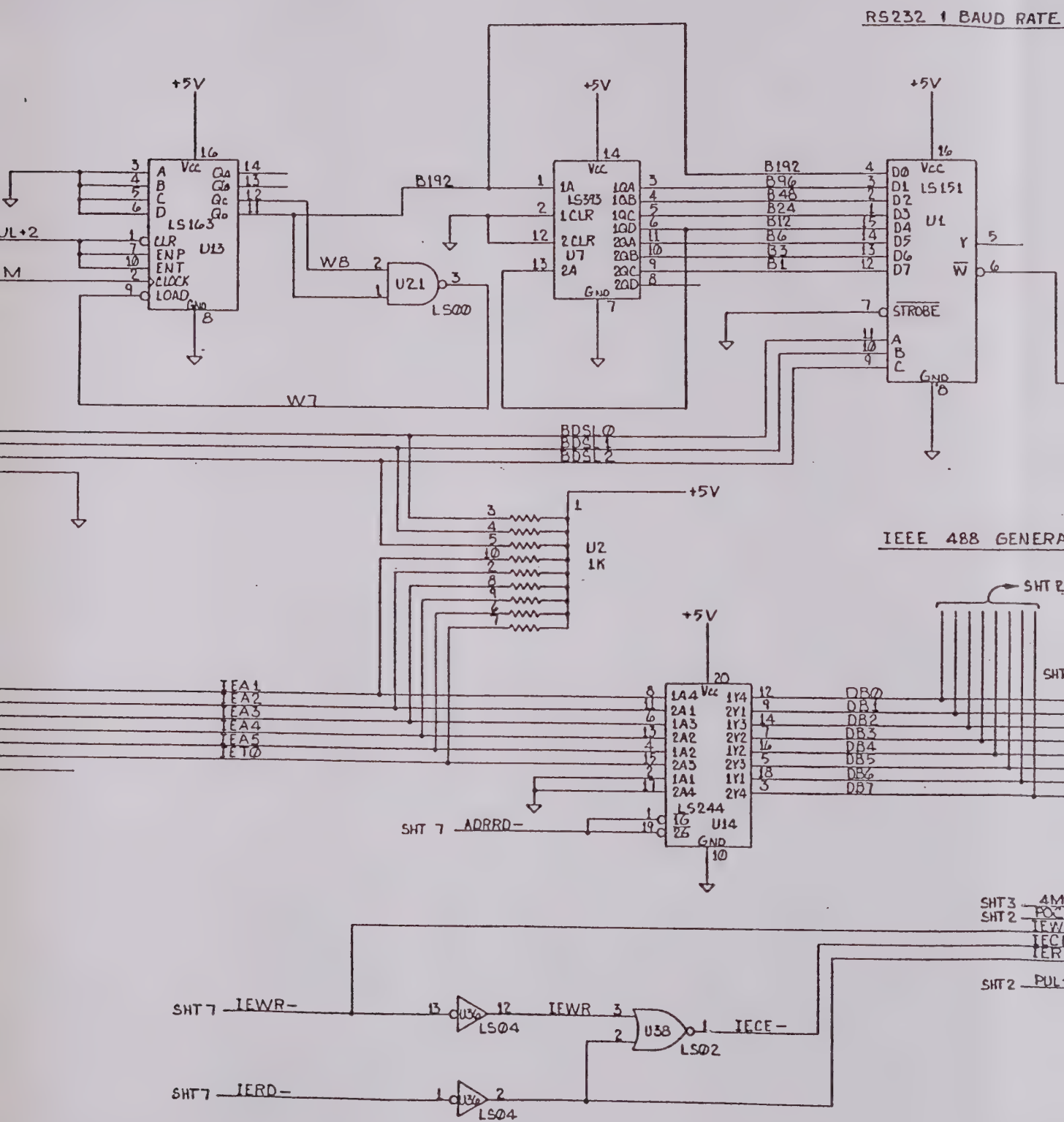

| | | | |
|---|---|---|---|
| interface TECHNOLOGY | | | |
| SCALE: | APPROVED BY: | | DRAWN BY |
| DATE: 6-6-85 | | | REVISED |
| SCHEMATIC - CPU | | | |
| SHT 2 | 55613 | REV A | DRAWING NUMBER 20010016 |


MEMORY DECODING
+5V
+5V
+5V
+5V
U8
1K
R3
1K
U32
6
R17
1K
SHT 2
AB11
AB12
AB13
AB14
AB15
MREQ -
U29
ROM 1 -
RAM 1 -
USER PROM -
RAM 2
VDTEN -
ROM 2 -
ENCODER -
MBR -
SHT 6
SHT 6
SHT 6
SHT 6


+5V
LS139
U24
SHT 2
AB10
AB11
VDTEN -
VIDEN -
SHT 5
DECODER -
TRAP -

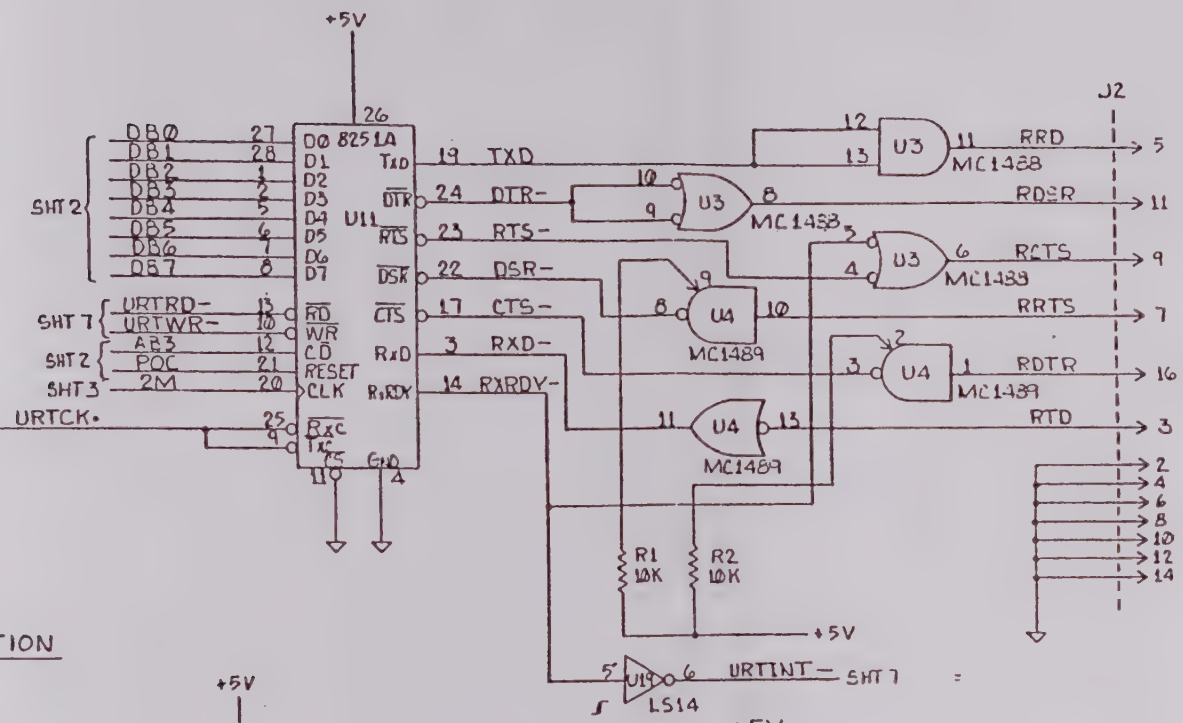

CLOCK GENERATION
+5V
C7
.1
C8
.1
MC12061
U17
8M
SHT 2
PUL+2
U18
LS74
SHT 2
PUL+2
AM
SHT 4
Y1
8MHZ


REVISIONS
LTR DATE APPR DESC
X0 SEE SHEET 1
A SEE SHEET 1
PART OF J4
USER PROM
4
PART OF J5
ENCODER-
DECODER-
TRAP-
PCLK
WAITR-
41
42
43
37
33
+5V
U32
LK
WTD-
WAITR-
U21
74LS00
U23
LS03
SHT2
PUL+2
U22
LS74
WAITP-
SHT 2
2M
SHT 4
R5
330
PCLK
U27
LS244
PCLK-
SHT 2
interface
TECHNOLOGY
SCALE:
DATE 6-6-85
APPROVED BY:
DRAWN BY
REVISED
SCHEMATIC - CPU
SHT 3
55613
REV A
DRAWING NUMBER
20010016

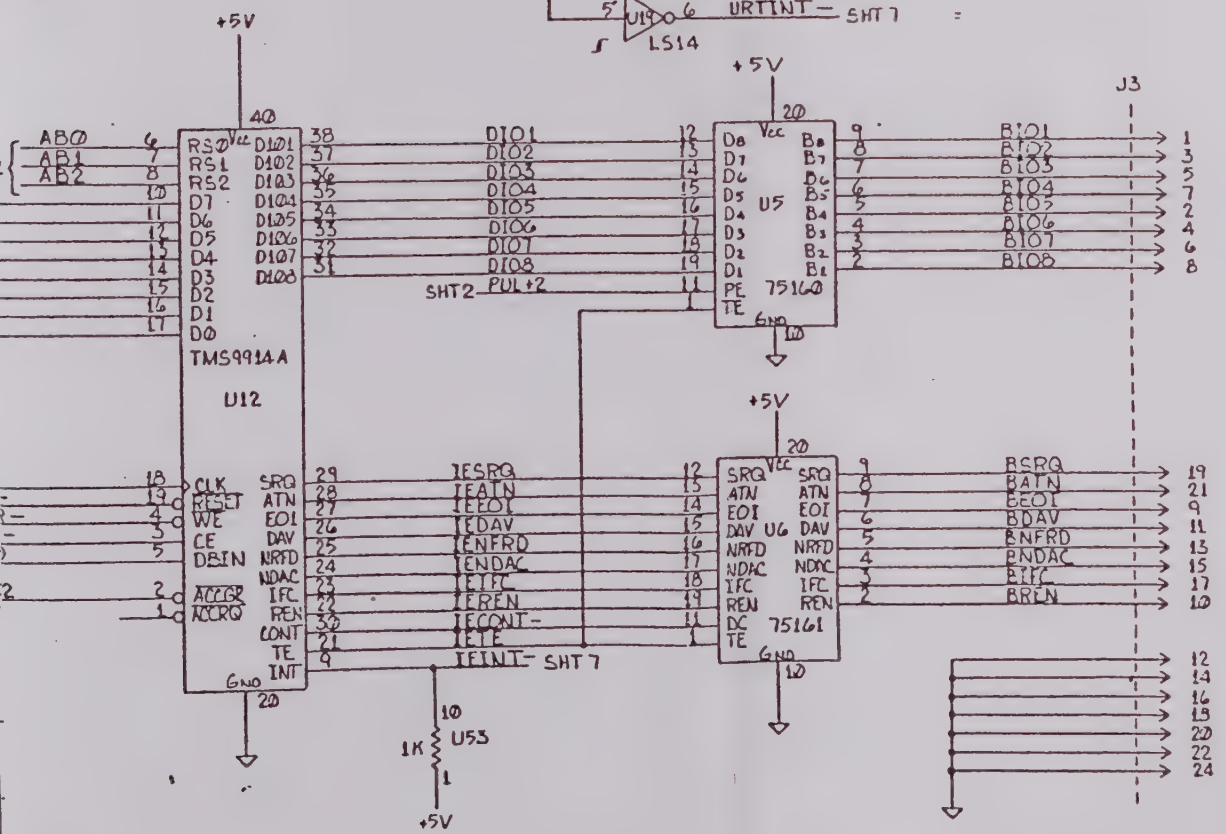

RS232 1 BAUD RATE
+5V
LS163
U13
LS393
U7
LS151
U1
B192
B96
B48
B24
B12
B6
B3
B1
WB
U21
LS00
W7
STROBE
BDSL0
BDSL1
BDSL2
U2
1K
IEEE 488 GENERA
SHT 8
SHT
IEA1
IEA2
IEA3
IEA4
IEA5
IETØ
LS244
U14
DBØ
DB1
DB2
DB3
DB4
DB5
DB6
DB7
SHT 7
ADRRD-
SHT3
SHT2
SHT2
SHT7
IEWR-
U36
LS04
IEWR
U38
LS02
IECE-
IERD-

| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APPR | DESCRIPTION |
| XO | | | SEE SHEET 1 |
| A | | | SEE SHEET 1 |

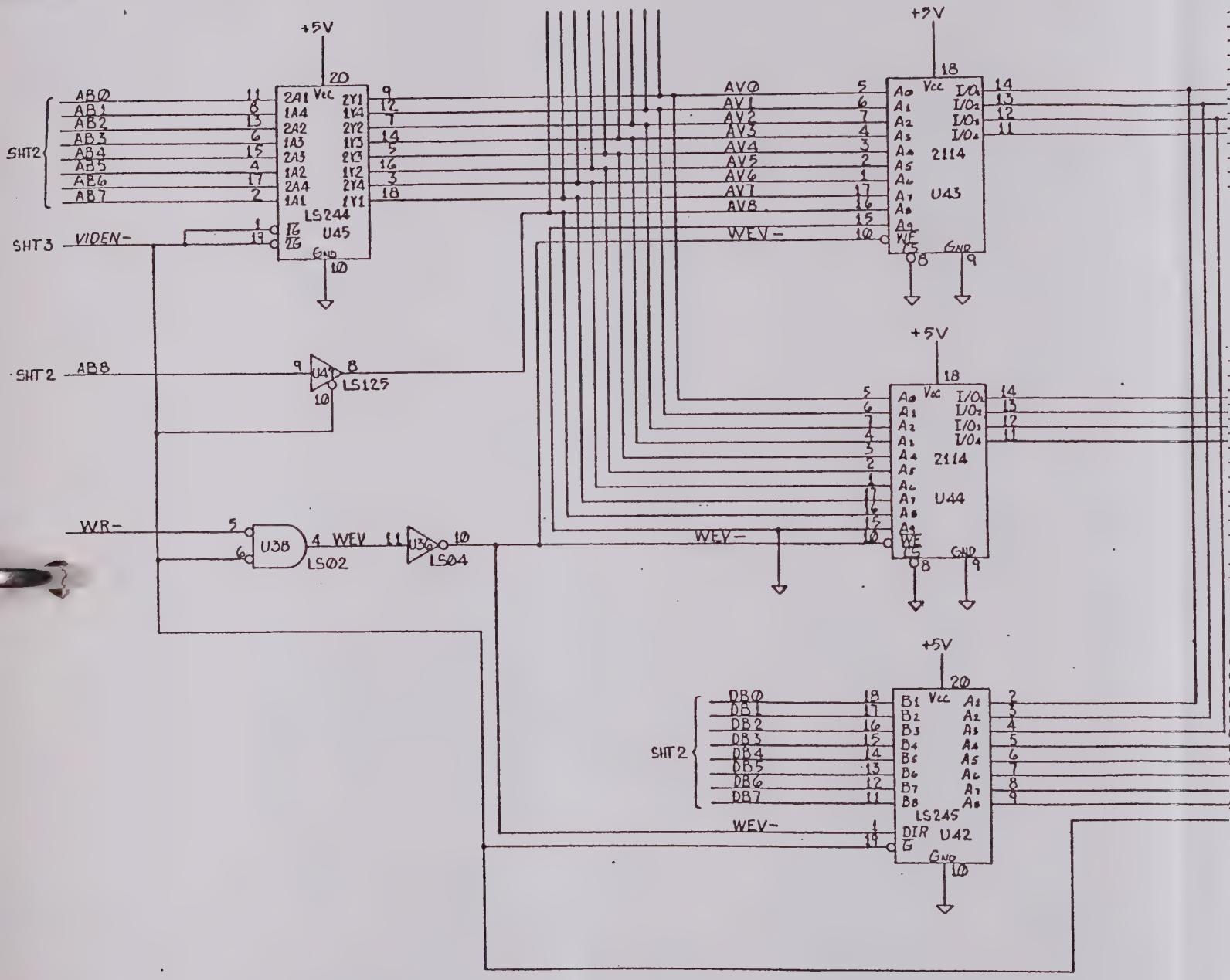
ENERATION

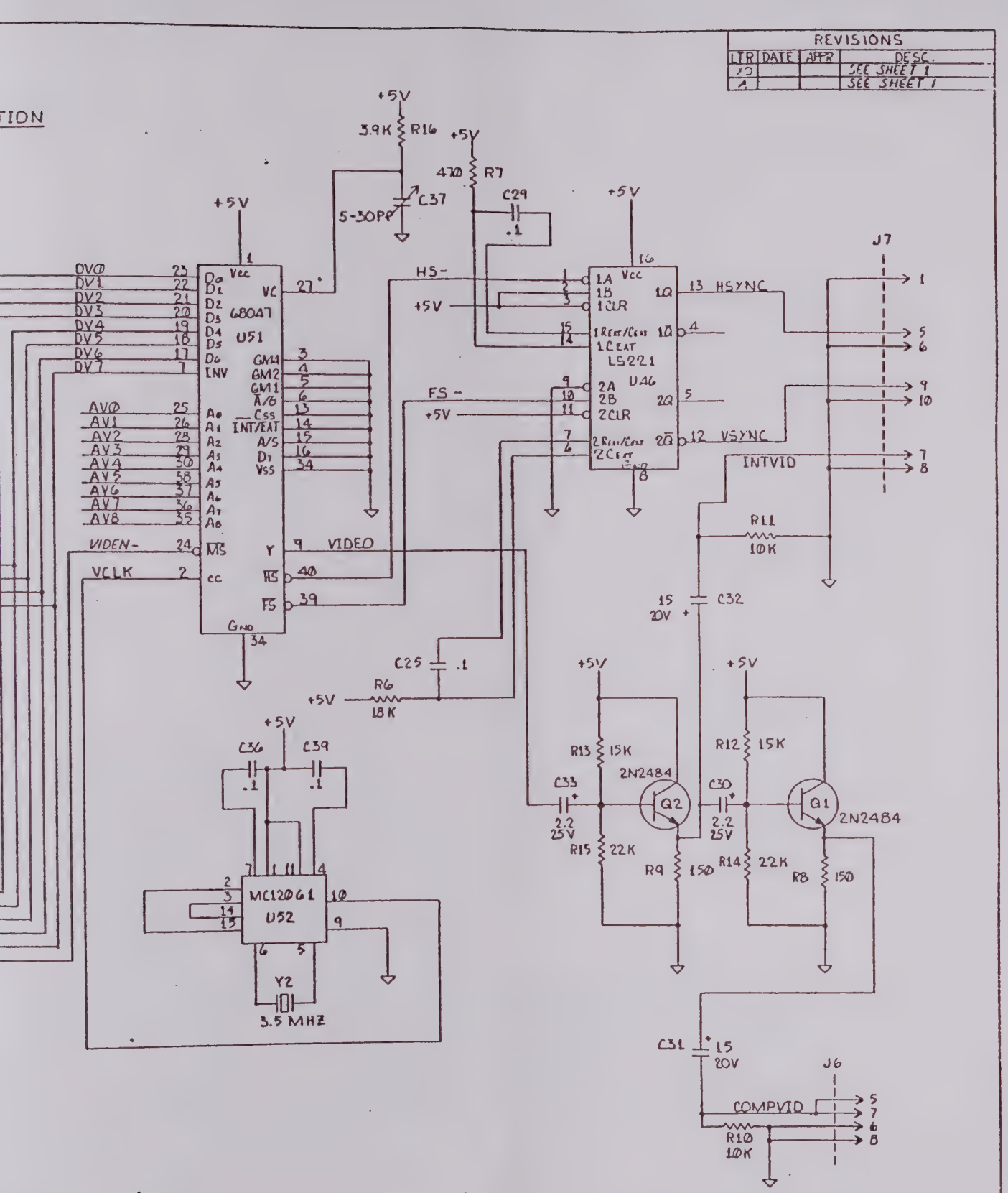


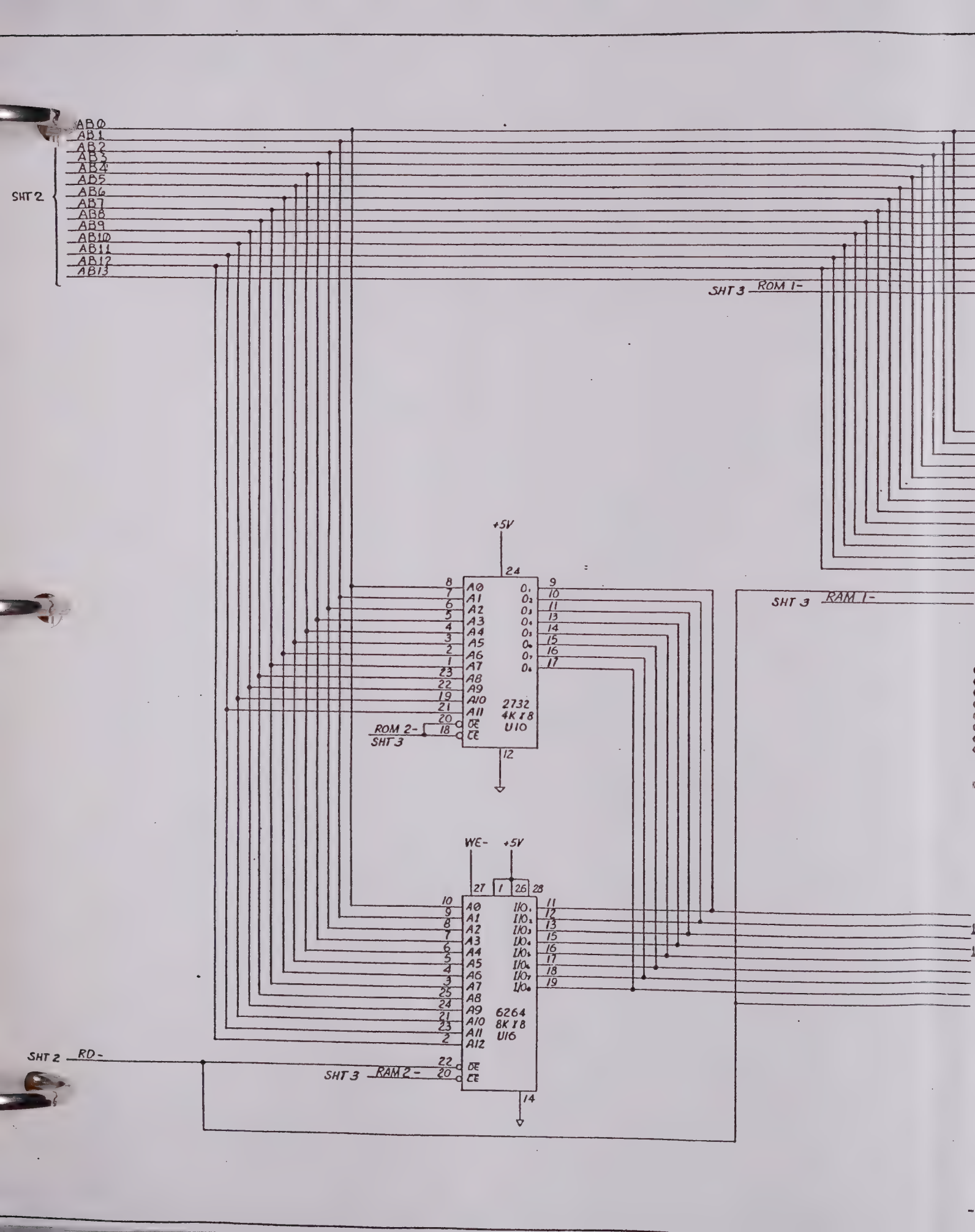

TION

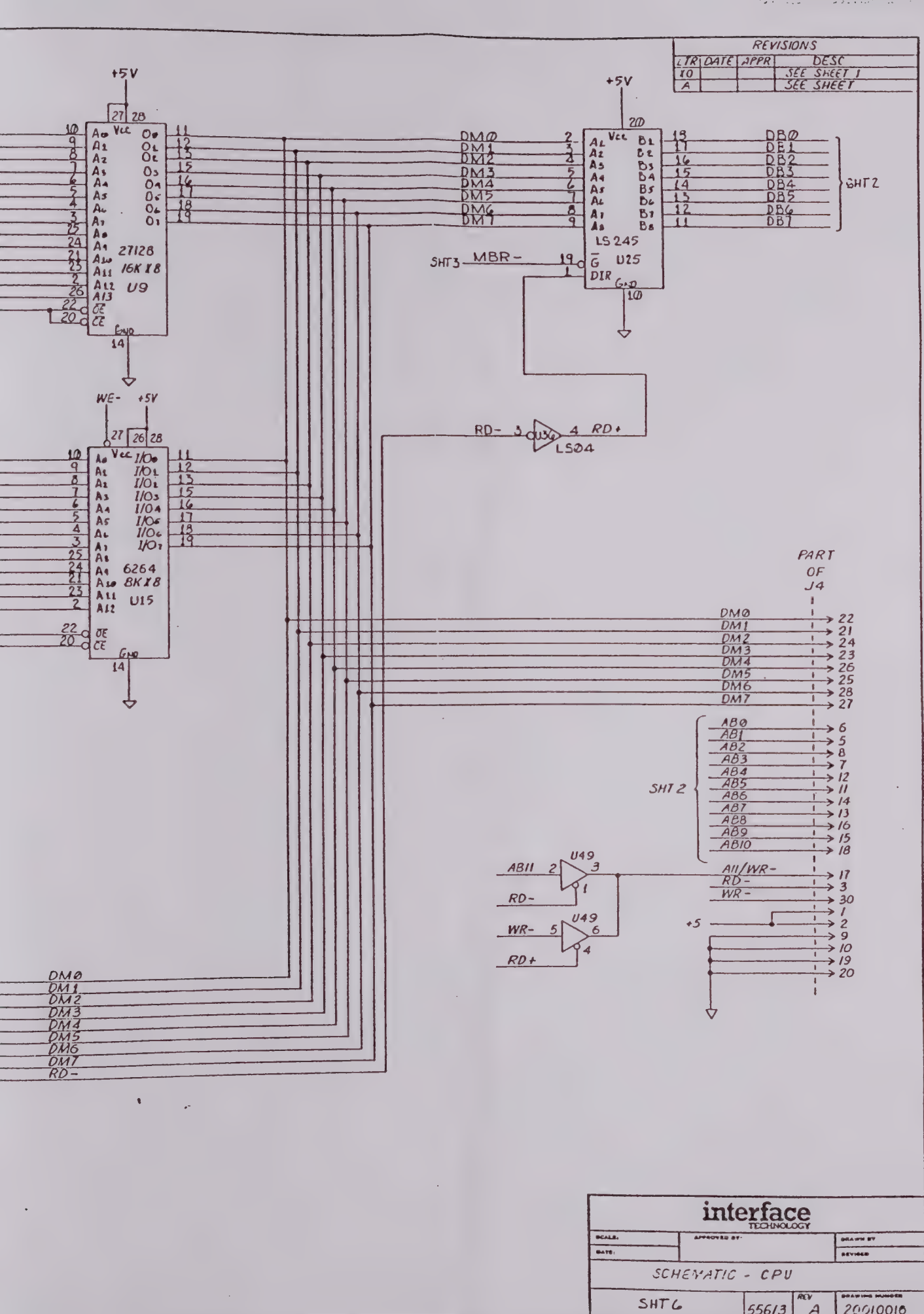

+5V
U12 TMS9914A
ABØ AB1 AB2
DIO1 DIO2 DIO3 DIO4 DIO5 DIO6 DIO7 DIO8
SHT2 PUL+2
U5 75160
BIO1 BIO2 BIO3 BIO4 BIO5 BIO6 BIO7 BIO8
J3
IESRQ IEATN IEEOI IEDAV IENFRD IENDAC IEIFC IEREN IECONT- IETE IEINT- SHT 7
U6 75161
BSRQ BATN BEOI BDAV BNFRD BNDAC BIFC BREN
1K U53

| | | | |
|---|---|---|---|
| interface TECHNOLOGY | | | |
| SCALE: | APPROVED BY: | | DRAWN BY |
| DATE: 6-6-85 | | | REVISED |
| SCHEMATIC – CPU | | | |
| SHT 4 | 55613 | REV A | DRAWING NUMBER 20010016 |

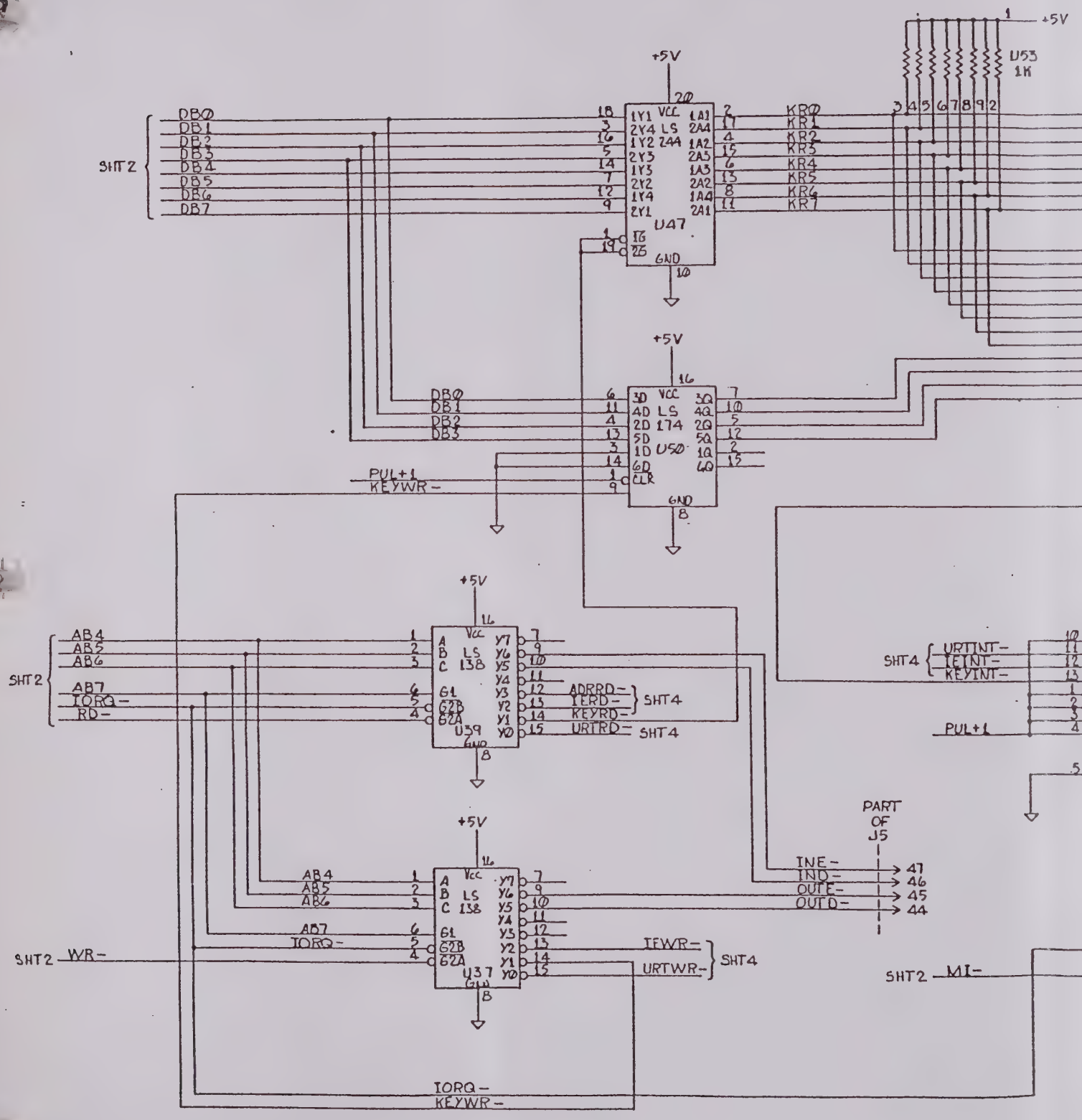

+5V
20
ABØ
AB1
AB2
AB3
AB4
AB5
AB6
AB7
SHT2
2A1 Vcc 2Y1
1A4 1Y4
2A2 2Y2
1A3 1Y3
2A3 2Y3
1A2 1Y2
2A4 2Y4
1A1 1Y1
LS244
1G 2G U45
GND
10
SHT3
VIDEN-
AB8
SHT2
U41
LS125
WR-
U38
LS02
WEV
U39
LS04
WEV-
AVØ
AV1
AV2
AV3
AV4
AV5
AV6
AV7
AV8
WEV-
18
Vcc
2114
U43
GND
U44
DBØ
DB1
DB2
DB3
DB4
DB5
DB6
DB7
SHT2
B1 Vcc A1
B2 A2
B3 A3
B4 A4
B5 A5
B6 A6
B7 A7
B8 A8
LS245
DIR U42
G
GND
WEV-


REVISIONS
LTR DATE APPR DESC
SEE SHEET 1
SEE SHEET 1
TION
+5V
3.9K R16
470 R7
5-30PF C37
C29 .1
U51 68047
U46 LS221
MC12061 U52
Y2 3.5 MHZ
R6 18K
C25 .1
C36 .1
C39 .1
R11 10K
C32 15 20V
C33 2.2 25V
C30 2.2 25V
C31 15 20V
R13 15K
R12 15K
R15 22K
R14 22K
R9 150
R8 150
2N2484
Q2
Q1
J7
J6
HS-
FS-
INTVID
VIDEO
COMPVID
R10 10K
VIDEN-
VCLK
interface TECHNOLOGY
SCALE:
DATE: 6-6-85
APPROVED BY:
DRAWN BY
REVISED
SCHEMATIC - CPU
SHT 5
55613
REV A
2001005

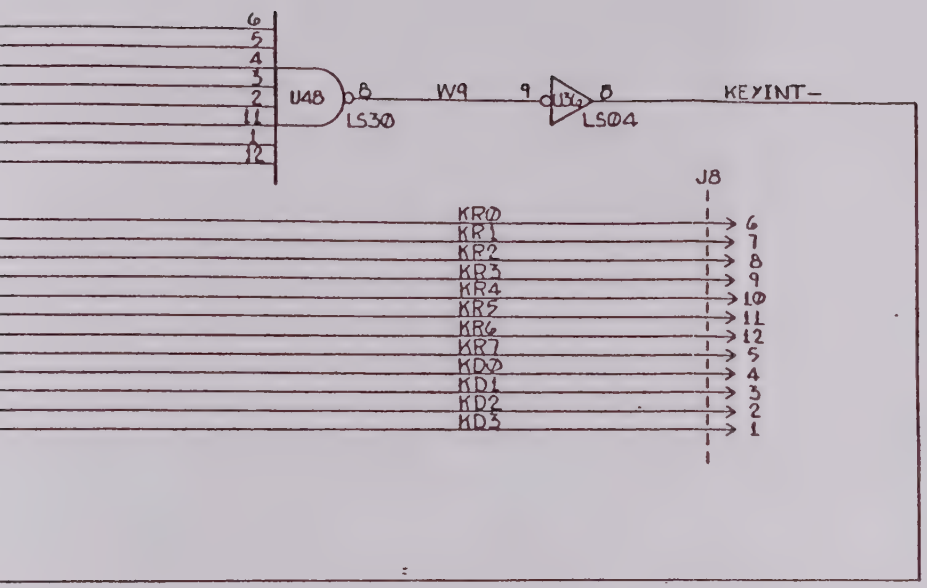

AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
AB12
AB13
SHT 2
SHT 3 ROM 1-
SHT 3 RAM 1-
+5V
24
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
OE
CE
O1
O2
O3
O4
O5
O6
O7
O8
2732
4K X 8
U10
ROM 2-
SHT 3
WE-
+5V
27
1
26
28
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
6264
8K X 8
U16
A12
SHT 2 RD-
SHT 3 RAM 2-

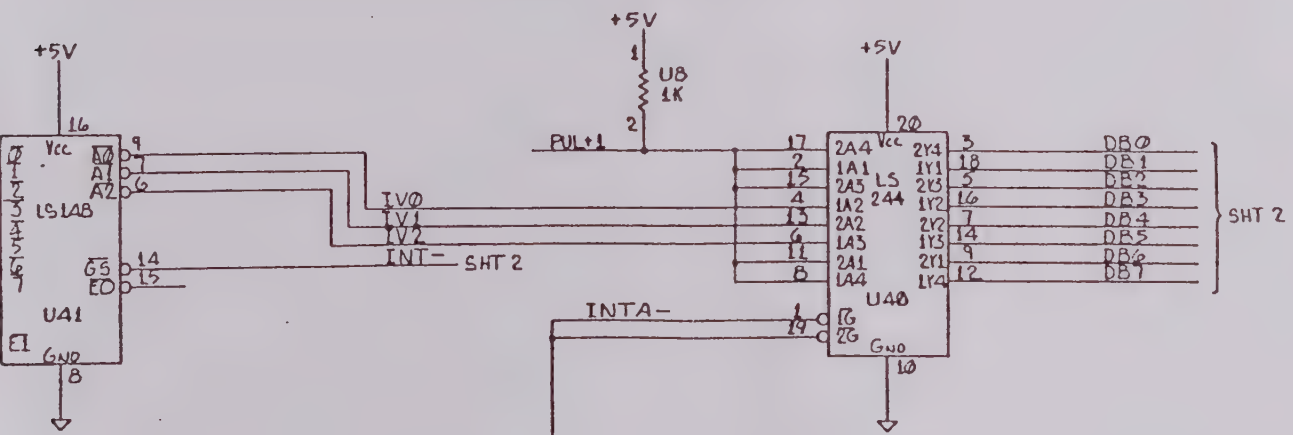



| | | | |
|---|---|---|---|
| interface TECHNOLOGY | | | |
| SCALE: | APPROVED BY: | | DRAWN BY |
| DATE: | | | REVISED |
| SCHEMATIC - CPU | | | |
| SHT 6 | 55613 | REV A | DRAWING NUMBER 20010016 |


+5V
U53
1K
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
SHT2
U47
KR0
KR1
KR2
KR3
KR4
KR5
KR6
KR7
GND
U50
PUL+1
KEYWR-
AB4
AB5
AB6
AB7
IORQ-
RD-
U39
ADRRD-
IERD-
KEYRD-
URTRD-
SHT4
URTINT-
IEINT-
KEYINT-
PART
OF
J5
INE-
IND-
OUTE-
OUTD-
U37
IEWR-
URTWR-
WR-
MI-

| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APPR | DESC. |
| XO | | | SEE SHEET 1 |
| A | | | SEE SHEET 1 |



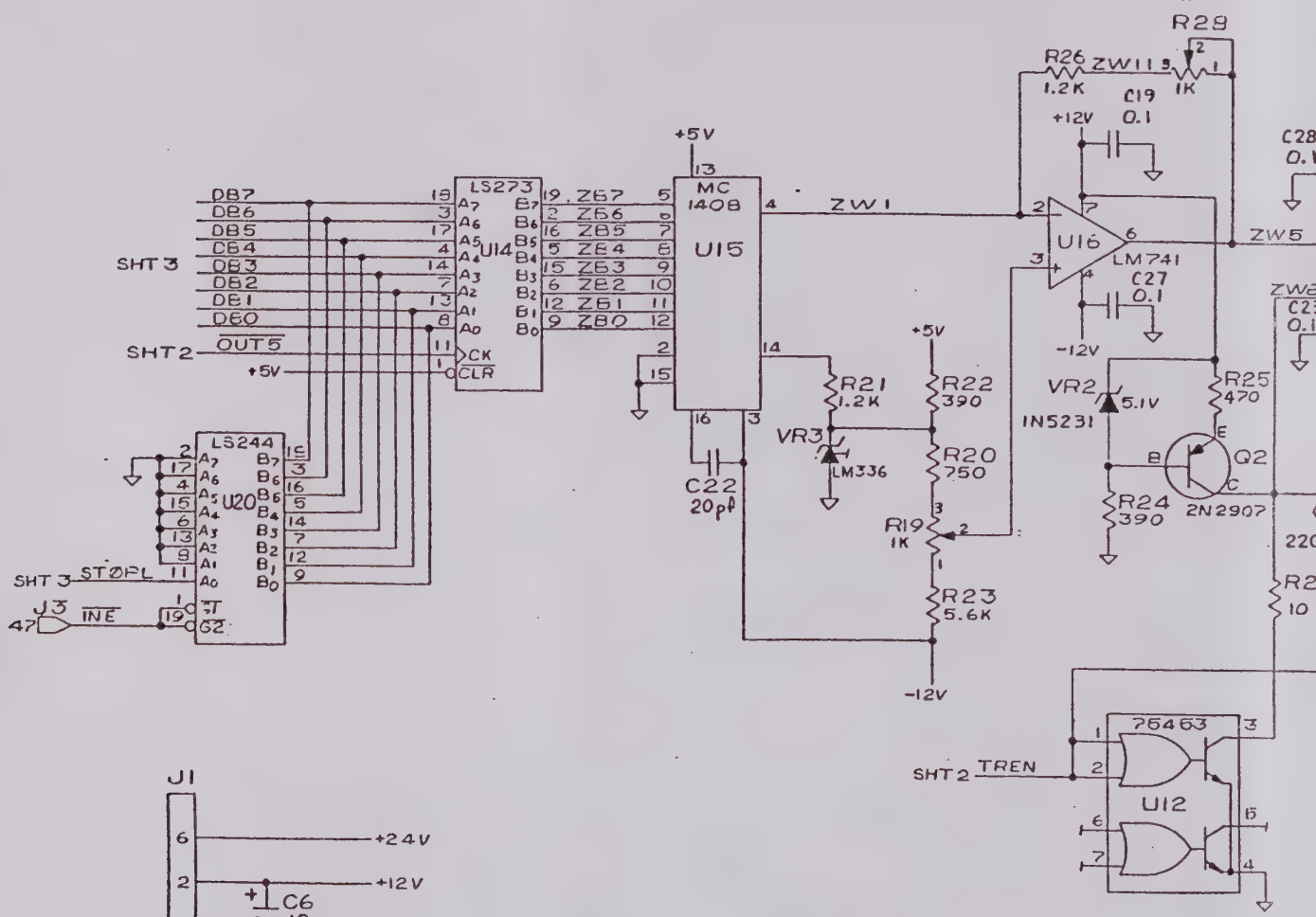



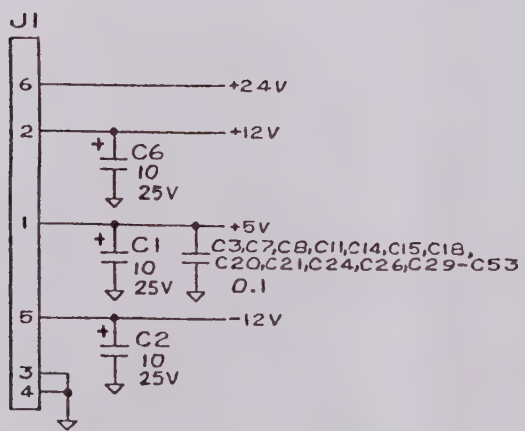
| interface TECHNOLOGY | | | |
|---|---|---|---|
| SCALE: | APPROVED BY: | | DRAWN BY |
| DATE 6-6-85 | | | REVISED |
| SCHEMATIC - CPU | | | |
| SHT 7 | 55613 | REV A | DRAWING NUMBER 20010016 |

NOTES: UNLESS OTHERWISE SPECIFIED

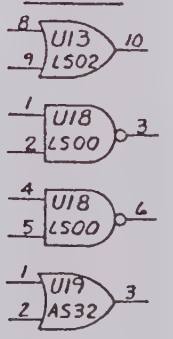
1. REFERENCE: CIRCUIT CARD ASSY NO 20010002.
2. ALL RESISTANCE VALUES ARE IN OHMS, 1/4W, ±10%.
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS, 50V.
4. DIODES ARE IN4148.

VARIABLE ZERØ CRØSSING SHIFTER



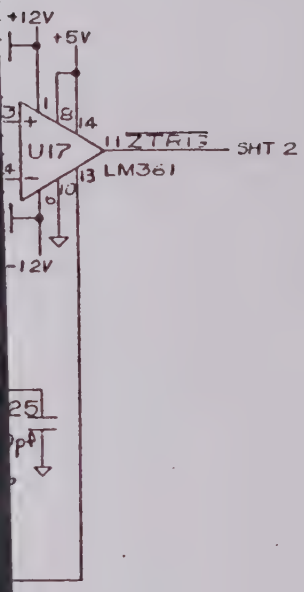



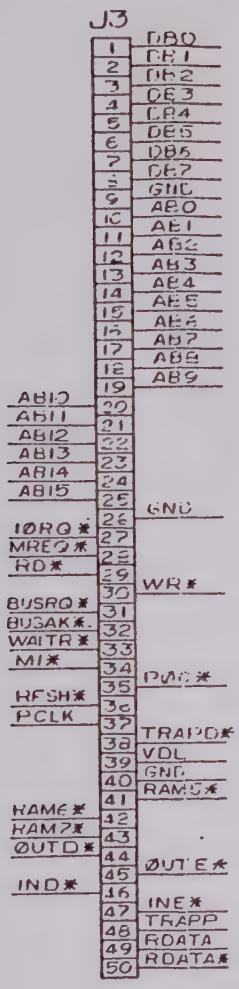

SPARES



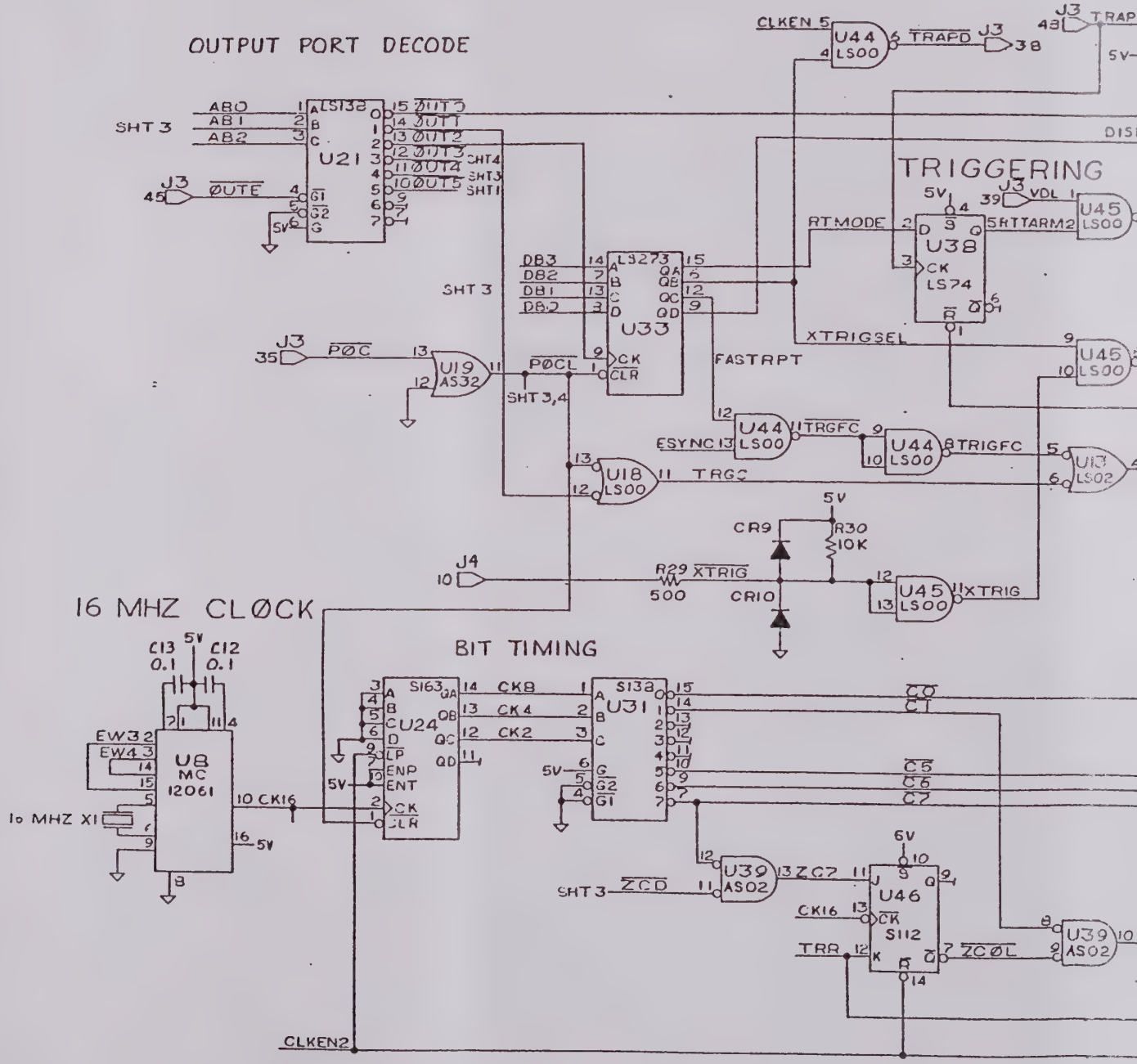

| LAST USED REFERENCE | NOT USED DESIGNATIONS |
|---|---|
| X1 | — |
| VR3 | — |
| U47 | — |
| TP3 | — |
| T4 | — |
| R30 | — |
| Q2 | — |
| K8 | — |
| J4 | — |
| CR10 | — |
| C54 | — |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APP'K | DESC |
| A | 6-28-85 | | PRODUCTION RELEASE |

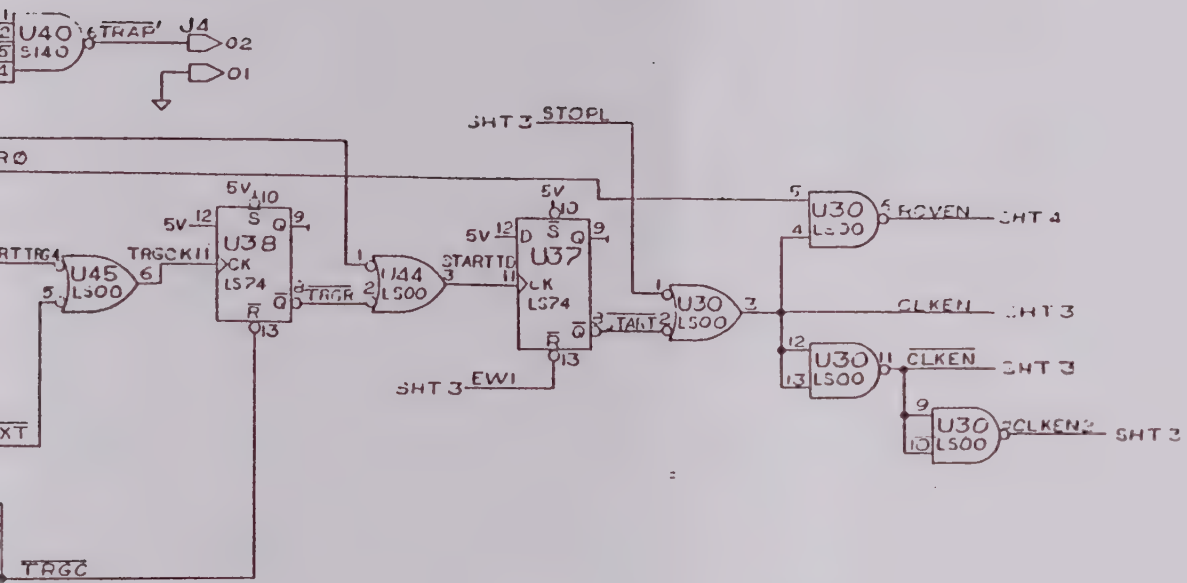


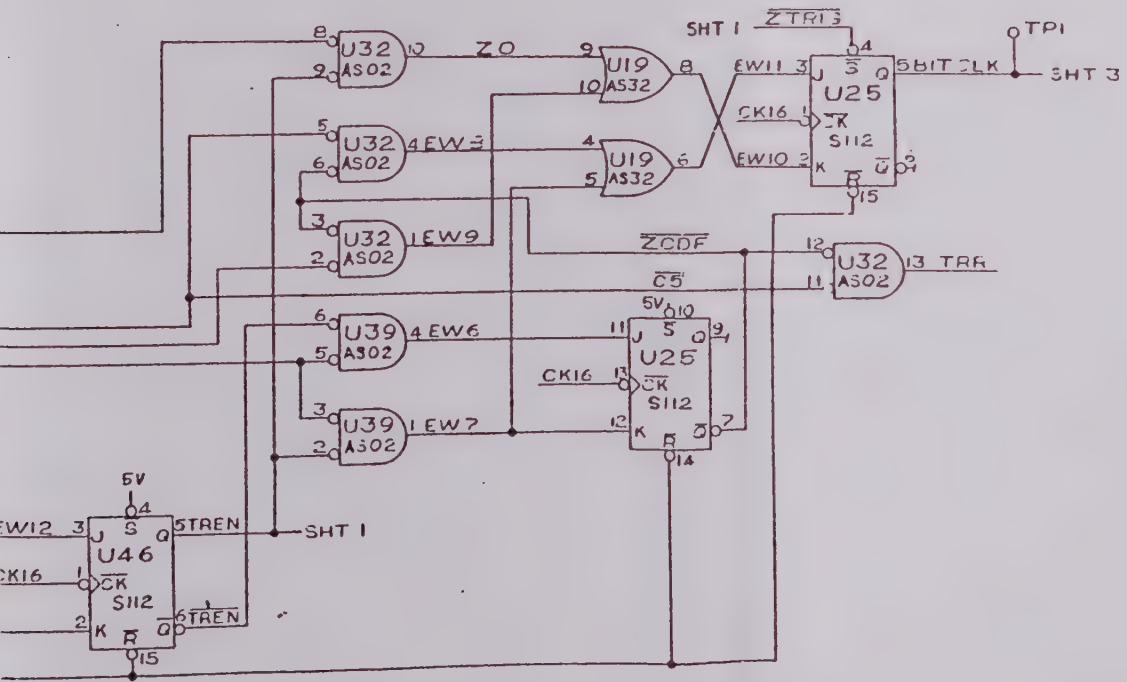




| | | | | | |
|---|---|---|---|---|---|
| interface TECHNOLOGY | | | | | |
| SCALE: NONE | APPROVED BY: | | | | DRAWN BY KAR |
| DATE: 6-28-85 | | | | | REVISED |
| 20010017 | MODEL 553A | SCHEMATIC - ENCODER | | | |
| NEXT ASSY | USED ON | | | | |
| APPLICATION | | SHT. 1 OF 4 | 55613 | REV A | DRAWING NUMBER 20010004 |

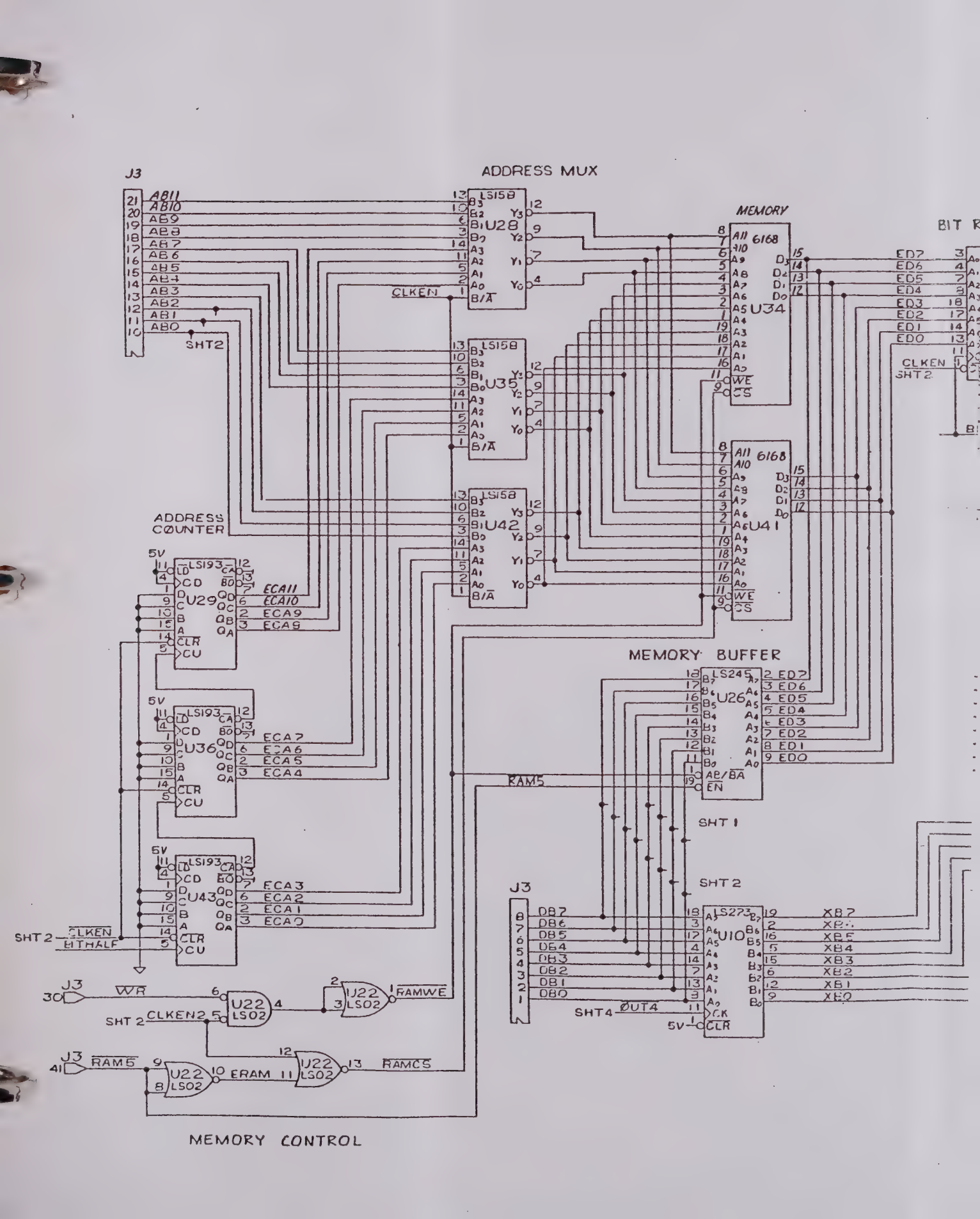

OUTPUT PORT DECODE
TRIGGERING
16 MHZ CLØCK
BIT TIMING
U21
LS138
U33
LS273
U38
LS74
U8
MC
12061
U24
S163
U31
S138
U46
S112
U44
LS00
U45
LS00
U18
LS00
U19
AS32
U39
AS02
SHT 3
ABØ
AB1
AB2
ØUTE
PØC
PØCL
SHT 3,4
DB3
DB2
DB1
DB0
FASTRPT
XTRIGSEL
RTMODE
TRAPD
TRGC
TRGFC
ESYNC
XTRIG
CR9
CR10
R30
10K
R29
500
C13
0.1
C12
0.1
10 MHZ XI
10 CK16
CKB
CK4
CK2
ENP
ENT
CLR
ZCD
ZC7
ZCØL
TRR
CKI6
CLKEN2
CLKEN 5
VDL 1
SRTTARM2
5V
6V

| ITR | DATE | APPR | REVISIONS |
|---|---|---|---|
| A | | | LESC SEE SHEET 1 |

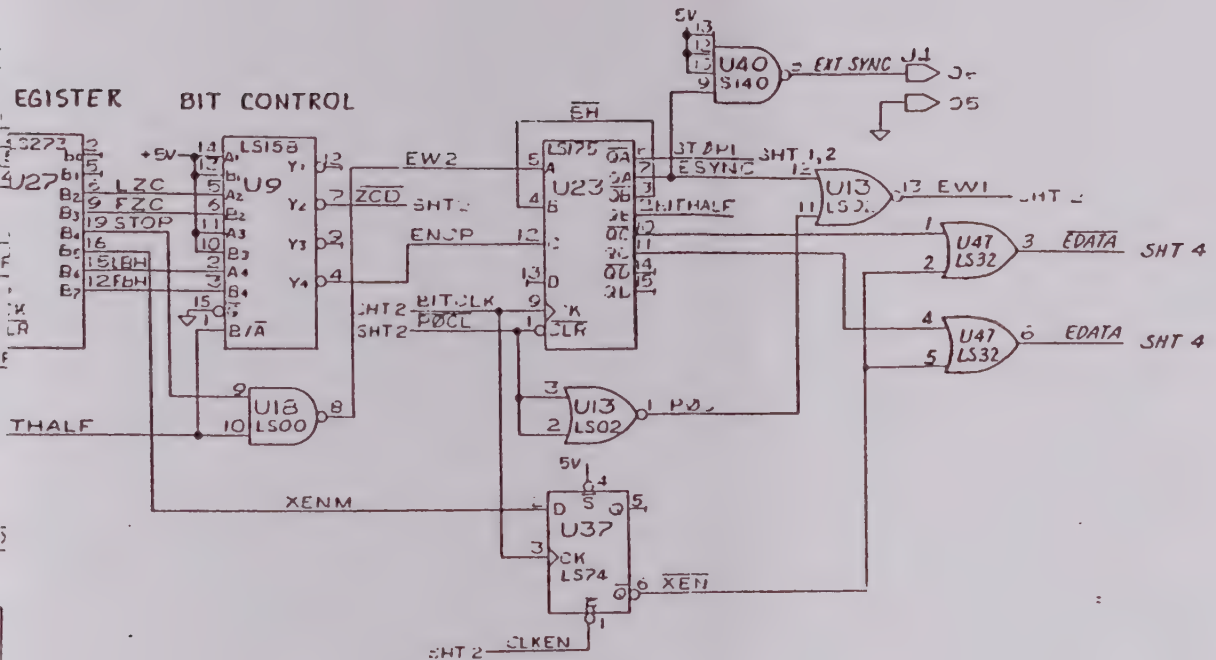


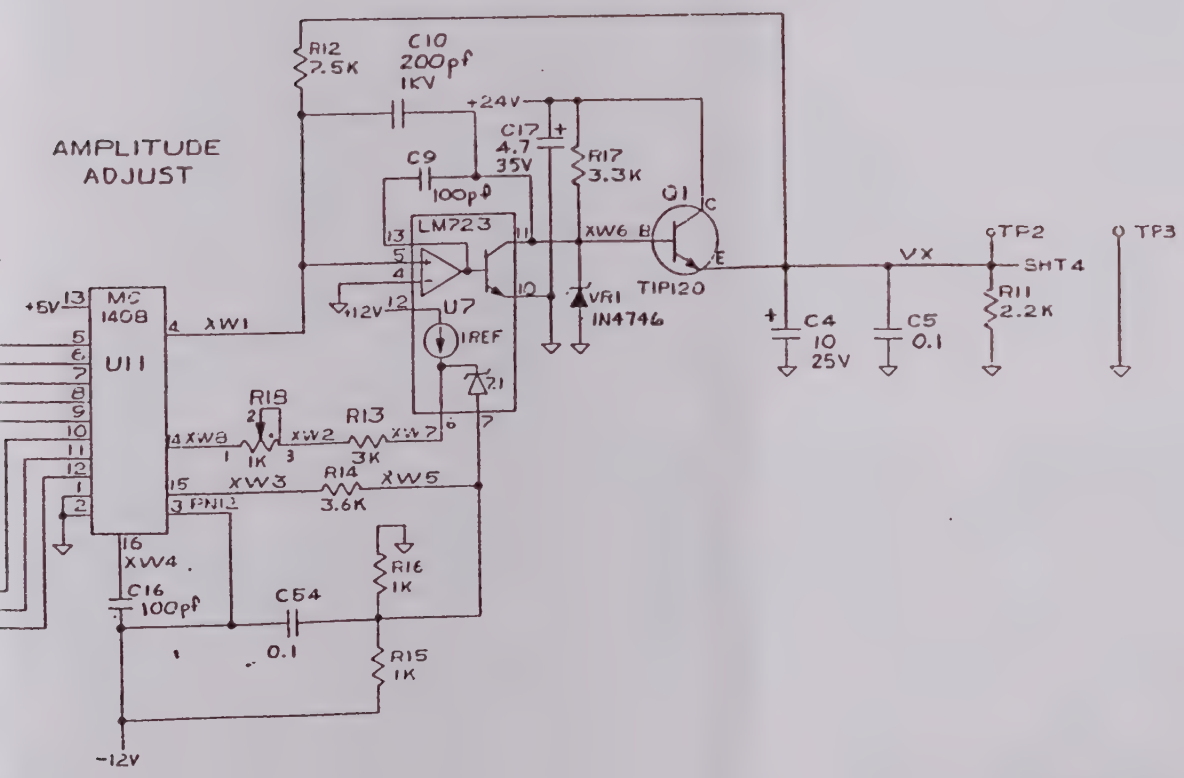




| interface TECHNOLOGY | | | |
|---|---|---|---|
| SCALE: NONE | APPROVED BY: | | DRAWN BY |
| DATE: | | | REVISED |
| SCHEMATIC - ENCODER | | | |
| SHT. 2 | 55613 | REV A | DRAWING NUMBER 20010004 |


J3
ADDRESS MUX
MEMORY
BIT R
AB11
AB10
AB9
AB8
AB7
AB6
AB5
AB4
AB3
AB2
AB1
AB0
SHT2
LS158
U28
U35
U42
CLKEN
A11 6168
U34
U41
ED7
ED6
ED5
ED4
ED3
ED2
ED1
ED0
ADDRESS
COUNTER
5V
LS193
U29
U36
U43
ECA11
ECA10
ECA9
ECA8
ECA7
ECA6
ECA5
ECA4
ECA3
ECA2
ECA1
ECA0
MEMORY BUFFER
LS245
U26
RAM5
SHT 1
SHT 2
J3
LS273
U10
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
XB7
XB6
XB5
XB4
XB3
XB2
XB1
XB0
SHT4
ØUT4
BITHALF
WR
CLKEN2
RAMWE
RAMCS
ERAM
U22
LS02
MEMORY CONTROL

| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APPR | DESC |
| A | | | SEE SHEET 1 |



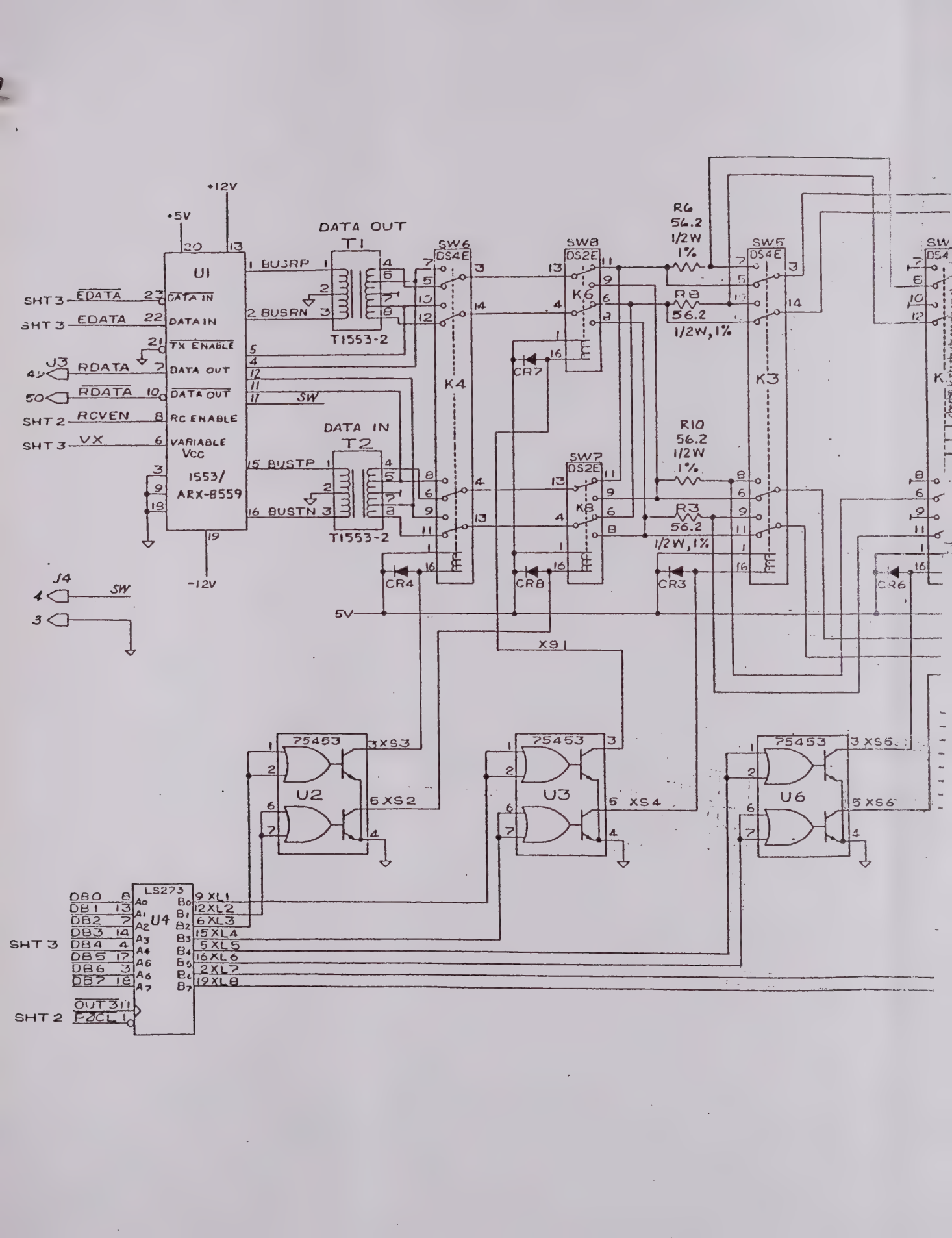




interface TECHNOLOGY

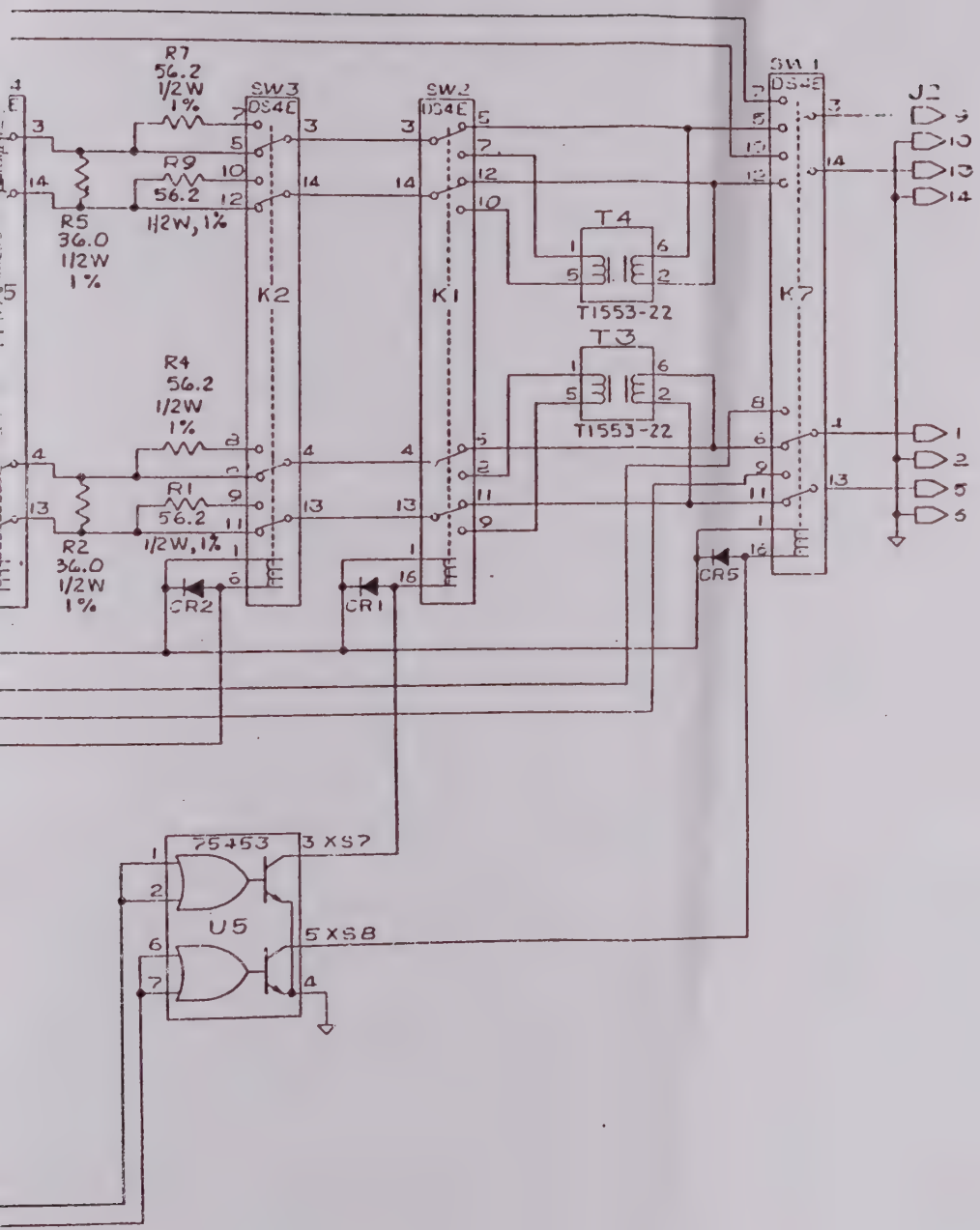
| | | | |
|---|---|---|---|
| SCALE: NONE | APPROVED BY: | | DRAWN BY |
| DATE: | | | REVISED |

SCHEMATIC - ENCODER

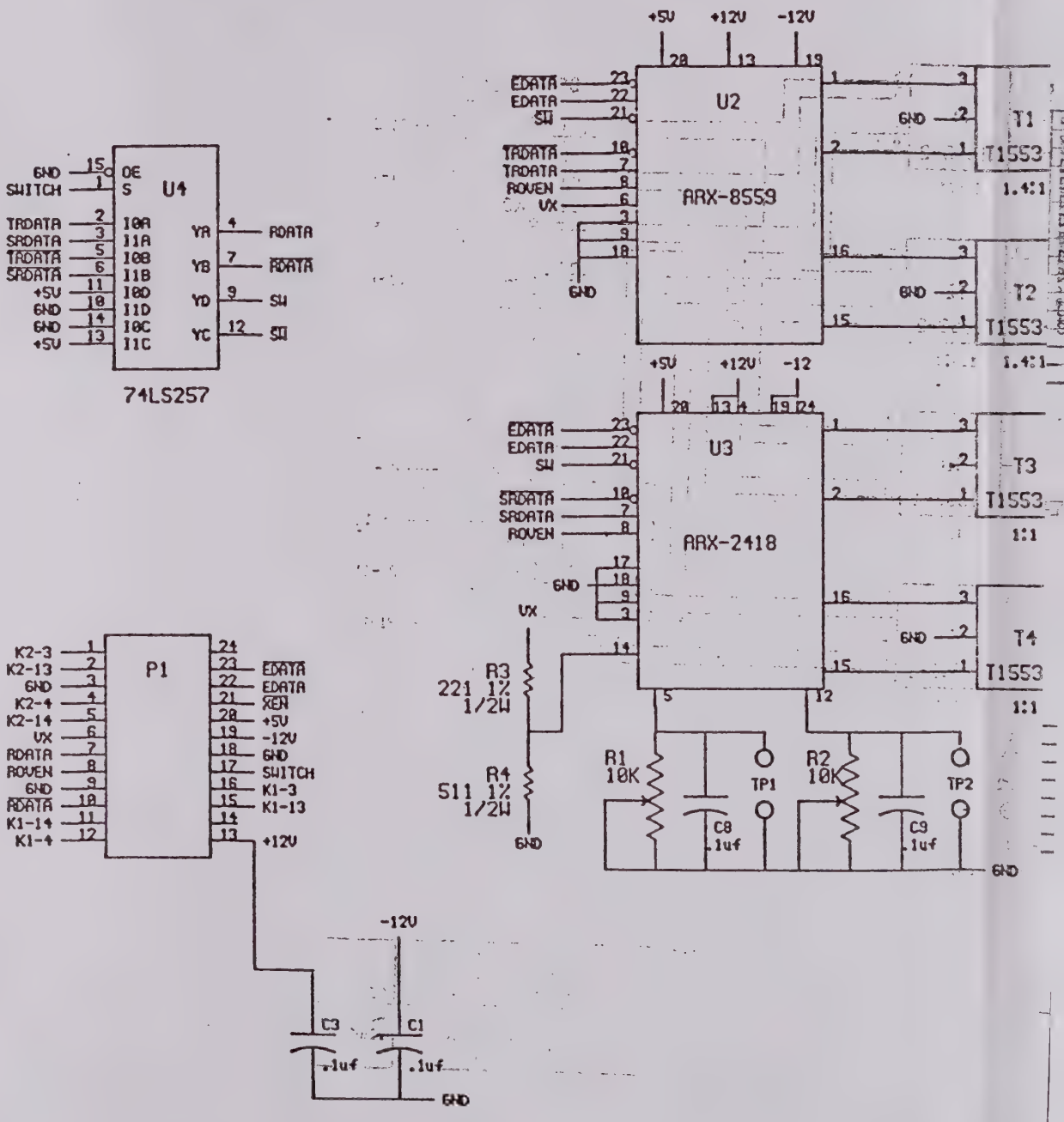
| | | | |
|---|---|---|---|
| SHT. 3 | 55613 | REV A | DRAWING NUMBER 20010004 |

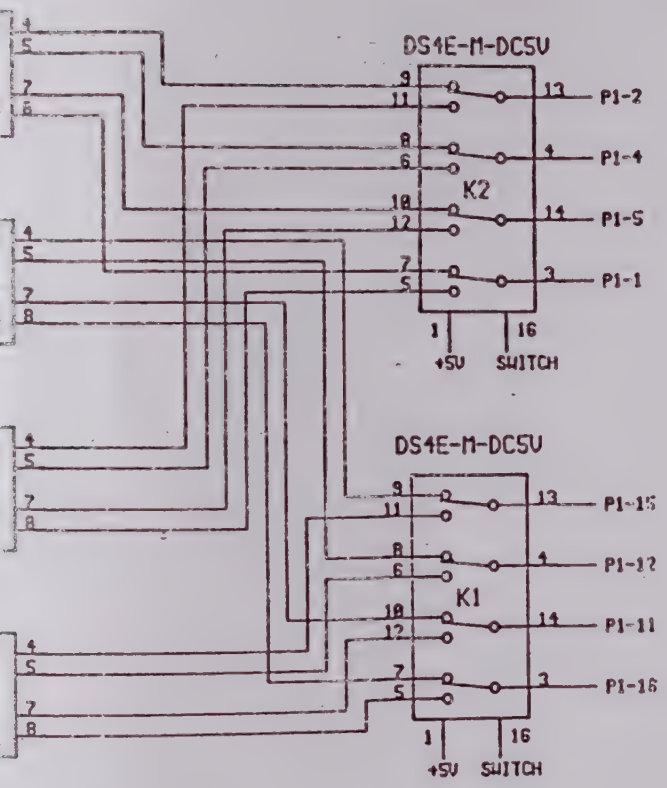

+12V
+5V
U1
1553/
ARX-8559
-12V
DATA OUT
T1
T1553-2
DATA IN
T2
T1553-2
SW6
SW8
SW5
K4
K6
K3
K8
SW7
CR7
CR4
CR8
CR3
CR6
R6
56.2
1/2W
1%
R8
56.2
1/2W,1%
R10
56.2
1/2W
1%
R3
56.2
1/2W,1%
5V
X91
J4
SW
U2
U3
U6
75453
3XS3
6XS2
XS4
3XS6
5XS6
U4
LS273
SHT 3
SHT 2
EDATA
RDATA
RCVEN
VX
BUSRP
BUSRN
BUSTP
BUSTN
TX ENABLE
RC ENABLE
VARIABLE Vcc
DATA IN
DATA OUT
SW
OUT311
P2CL1
9XL1
12XL2
6XL3
15XL4
5XL5
16XL6
2XL7
19XL8

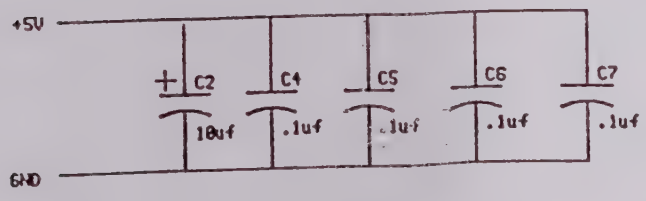
| REVISIONS | | | |
|---|---|---|---|
| LTR | DATE | APPR | DESC |
| A | | | SEE SHEET 1 |



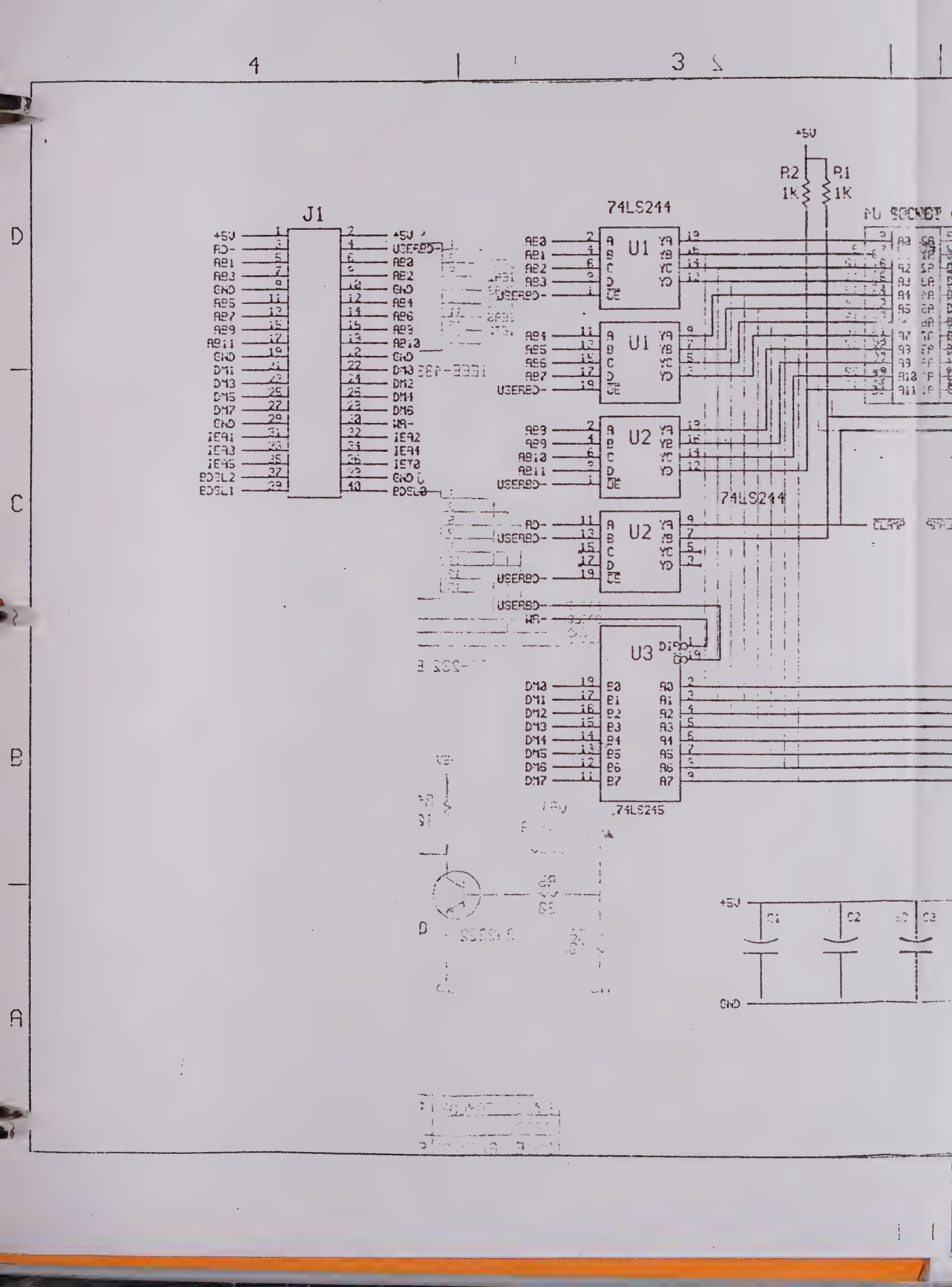

| interface TECHNOLOGY | | | |
|---|---|---|---|
| SCALE: NONE | APPROVED BY: | | DRAWN BY |
| DATE: | | | DESIGNED |
| SCHEMATIC - ENCODER | | | |
| SHT. 4 | 55613 | REV A | DRAWING NUMBER 20010C04 |

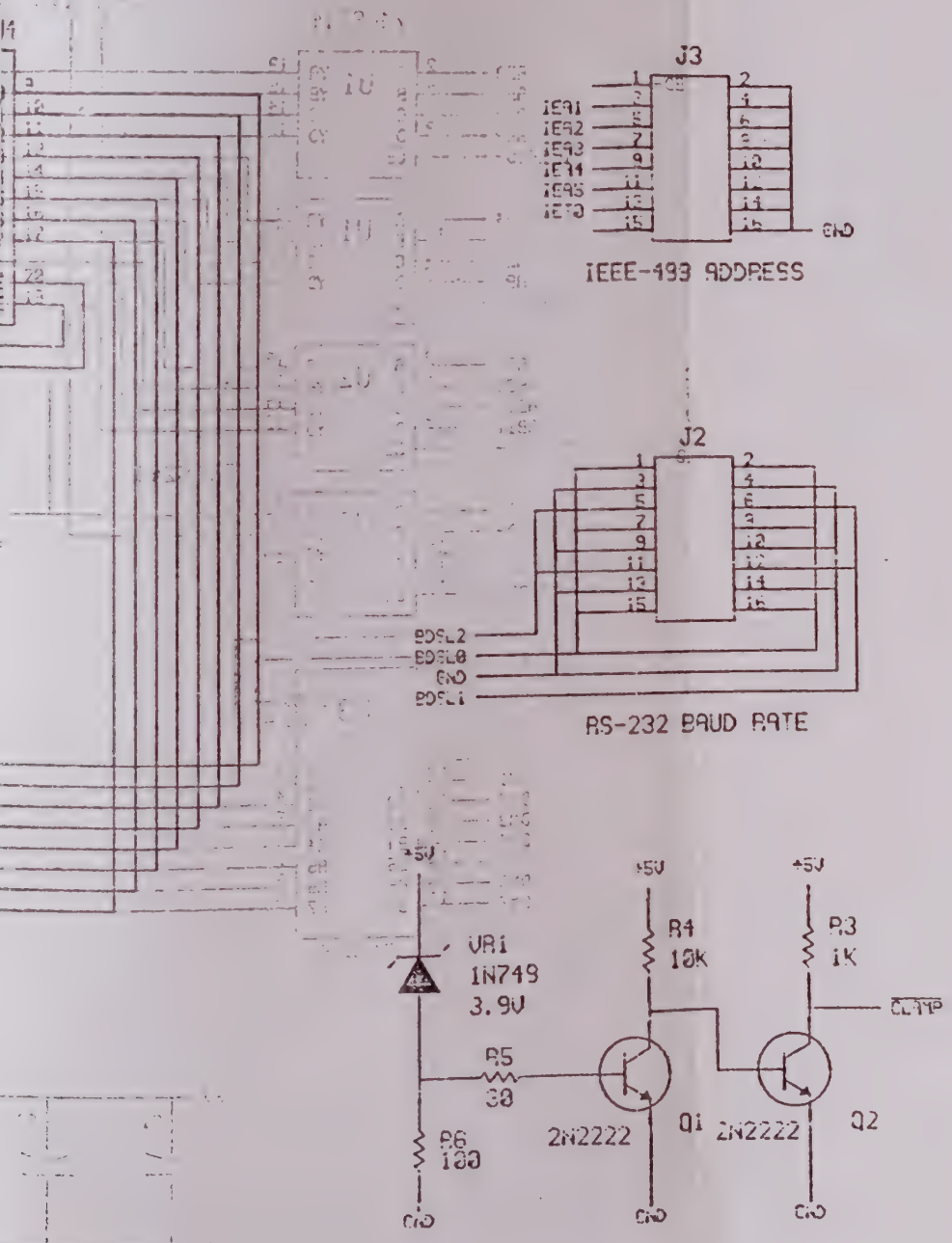

4
3
D
C
B
A
U4
74LS257
GND
SWITCH
TRDATA
SRDATA
TRDATA
SRDATA
+5V
GND
GND
+5V
OE
S
I0A
I1A
I0B
I1B
I0D
I1D
I0C
I1C
YA
YB
YD
YC
RDATA
RDATA
SW
SW
P1
K2-3
K2-13
GND
K2-4
K2-14
VX
RDATA
ROVEN
GND
RDATA
K1-14
K1-4
EDATA
EDATA
XEN
+5V
-12V
GND
SWITCH
K1-3
K1-13
+12V
U2
ARX-8559
+5V
+12V
-12V
EDATA
EDATA
SW
TRDATA
TRDATA
ROVEN
VX
GND
T1
T2
T1553
1.4:1
U3
ARX-2418
+5V
+12V
-12
SRDATA
SRDATA
ROVEN
GND
T3
T4
T1553
1:1
VX
R3
221 1%
1/2W
R4
511 1%
1/2W
GND
R1
10K
R2
10K
TP1
TP2
C8
.1uf
C9
.1uf
GND
-12V
C3
.1uf
C1
.1uf
GND




| | | | |
|---|---|---|---|
| BY: D.TAYLOR | TITLE | SINE/TRAP BOARD | |
| APPR. | | | |
| DATE 9/17/95 | SHEET 1of 1 | REV. A | DWG.#20010008 |


J1
74LS244
U1
U2
U3
74LS245
+5V
R2
1K
R1
1K
GND
CLAMP




| | | | |
|---|---|---|---|
| R. D. TAYLOR | TITLE | 5539 USER BOARD | |
| APPR. | | | |
| DATE 6/23/35 | PAGE 1 OF 1 | REV. | DWG # 20010008 |

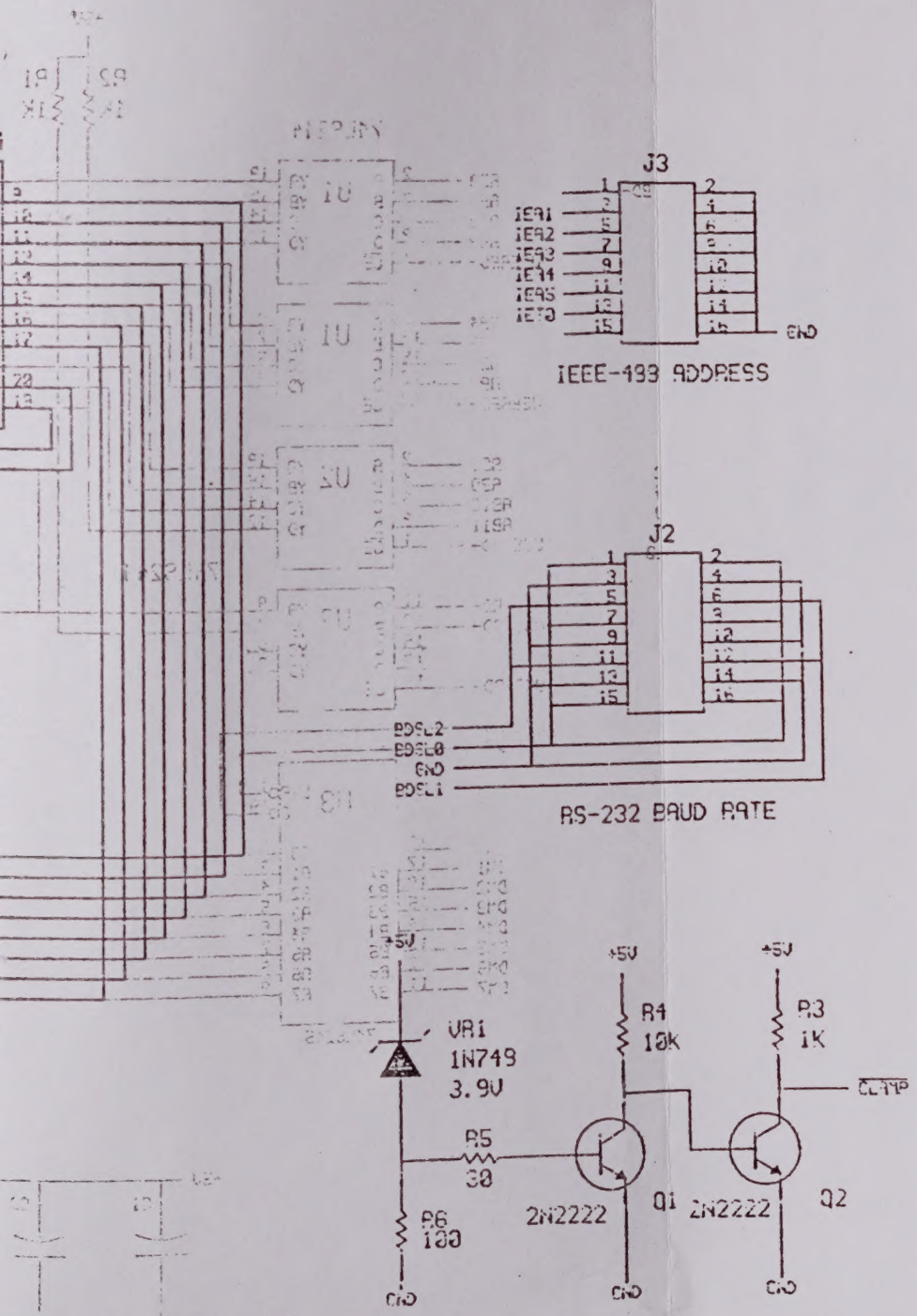
# Sundials & Timedials

GERALD JENKINS MAGDALEN BEAR

KQ-931-843

ISBN 0-906212-59-6

Tarquin




| | | | |
|---|---|---|---|
| BY D. TAYLOR | TITLE | 5539 USER BOARD | |
| APPR. | | | |
| DATE 6/23/35 | PAGE 1 OF 1 | REV. | DWG # 20010008 |